High-performance ZnO nanowire field effect transistors

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ZnO nanowires with high crystalline and optical properties are characterized, showing strong effect of the surface defect states. In order to optimize the performance of devices based on these nanowires, a series of complementary metal-oxide semiconductor compatible surface passivation procedures is employed. Electrical transport measurements demonstrate significantly reduced subthreshold swing, high on/off ratio, and unprecedented field effect mobility. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2357013]

Semiconducting nanowires and nanotubes have demonstrated promising potential as the building blocks for nanoscale electronics. As one of the fundamental functional components, field effect transistors (FETs) using these quasi-one-dimensional (Q1D) structures as active channels have been extensively investigated in the past years.[1–4] However, the optical and electrical transport characterizations on nanowire FETs have revealed that the surface defect states deteriorate the device performance in mobility, on/off ratio, and subthreshold swing.[5,6] This significantly hinders their application for high density and high speed Q1D-based circuits. In order to optimize the performance of the Q1D FETs, it is critical to passivate these surface states. In fact, organic coatings have been utilized to passivate the surface states of Si nanowires[2] and ZnO nanorods.[4] Although the reported carrier mobilities have been increased, the stability of the organic passivation layer is unclear. In this letter, we report high-performance device characteristics of ZnO nanowires after surface passivation using a complementary metal-oxide semiconductor (CMOS) compatible process.

ZnO nanowire has attracted tremendous interest due to its remarkable physical properties and versatile applications in electronics, including logic circuit,[7] UV emitter,[8,9] photodetector,[10] as well as chemical sensor.[5,11] In this work, single crystalline ZnO nanowires are synthesized via a vapor trapping chemical vapor deposition (CVD) method.[12] Structural characterization of the as-grown ZnO nanowires is performed by field emission scanning electron microscope (FE-SEM) and high resolution transmission electron microscope (HRTEM) analyses. FE-SEM image, as shown in Fig. 1(a), illustrates Q1D nanostructures on the silicon substrate. The TEM image [Fig. 1(b)] displays two ZnO nanowires initiated from Au catalysts, manifesting the vapor-liquid-solid catalytic growth mechanism.[13] A long straight ZnO nanowire is illustrated in Fig. 1(c). The HRTEM lattice resolved image [Fig. 1(d)] demonstrates the lattice spacing of 0.52 nm in accordance with the *c* lattice constant of ZnO, indicating that the nanowire growth direction is along the *c* axis. Selected area electron diffraction (SAED) pattern [inset of Fig. 1(d)] confirms the [0001] growth direction.

Photoluminescence (PL) measurements have been conducted by utilizing He–Cd laser ($\lambda = 325$ nm) incident excitation to illuminate the ZnO nanowires at various temperatures. Temperature dependence PL (12–295 K) spectra displayed in Fig. 2(a) clearly demonstrate the evolution of peak intensities resulted from different radiative mechanisms. At low temperatures, the intense sharp peak at 3.362 eV is attributed to donor bound excitons [labeled as D^0X in Fig. 2(a), commonly denoted as I_5], but its chemical and structural origin is yet clear.[14] The sharp line with its full width at half maximum of 3.6 meV at 12 K [in Fig. 2(b)] and the absence of other DX lines from I_0–I_{11} indicate that the nanowires are of high crystalline and optical qualities. On the low-energy side [best seen in the 100 K spectrum in Fig. 2(a)], there are two emerging peaks at 3.310 and 3.234 eV (denoted as X1 and X2) with increasing temperature. These peaks represent the longitudinal phonon (LO) replica of the free excitons (labeled as FX).[15] The redshift of the band gap and the broadening of the PL lines with increas-

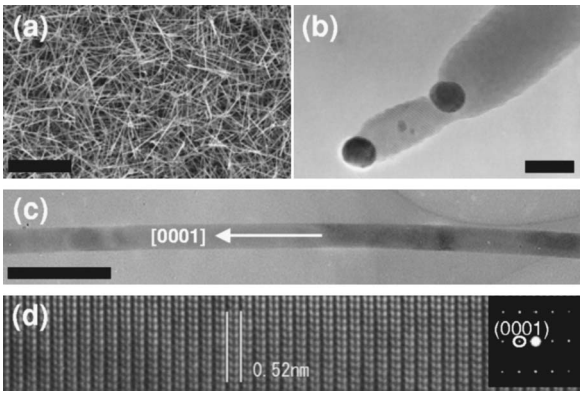

FIG. 1. (a) FE-SEM image shows the as-grown ZnO nanowires (scale bar is 10 μm). (b) TEM image displays two ZnO nanowires grown from the Au nanoparticle catalysts (scale bar is 15 nm). (c) A ZnO nanowire with diameter of 35 nm illustrates the high aspect ratio geometry (scale bar is 150 nm). (d) Lattice spacing is about 0.52 nm in the HRTEM image and the inset SAED indicates that the growth direction is [0001] along the *c* axis.

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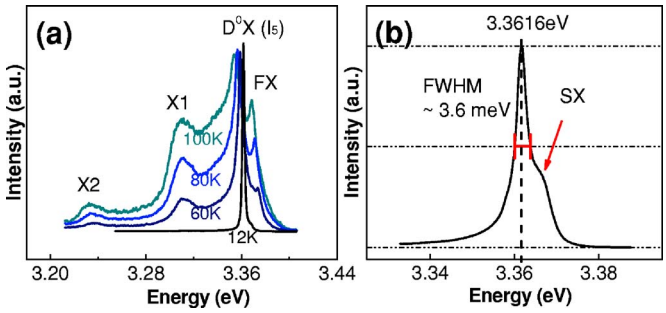

FIG. 2. (Color online) (a) Set of PL data displays the increasing free exciton (FX) luminescence peak and decreasing donor bound exciton (D^0X) peak with rising temperature. LO replica of the FX is observed at X1 and X2. (b) The high resolution PL of the band-edge luminescence, taken at 12 K, shows the sharp D^0X line as well as the surface bound exciton (SX).

ing temperature are results of the interaction of excitons with optical phonons and increased exciton thermal ionization.[16,17] The shoulder on the high-energy side [labeled as SX in Fig. 2(b)] originates from the recombination of surface excitons. This feature scales with the diameter[18] and reveals the presence of optically active surface states and confirms the high surface/volume ratio of the as-grown nanowires.

The as-synthesized ZnO nanowires are then fabricated into FETs. Nanowire suspension is first deposited on a silicon substrate, which consists of a thermally grown SiO_2 layer (500 nm thick) capped on p^{++} Si functioning as a back gate electrode. Photolithography technique is utilized to define metal leads onto the two ends of individual ZnO nanowires serving as the source and drain electrodes. To achieve Ohmic contact for attaining high device performance,[19,20] the metal leads composed of 10 nm titanium (Ti) adhesive layer and 100 nm gold (Au) are used. In order to investigate the uniformity of the nanowire channel, multiple electrodes have been defined on a nanowire with equal intervals of 4 μm, as shown in Fig. 3(a). The conductances across different channel segments are found to be proportional to the length [Fig. 3(b)], suggesting that the nanowire has high electrical uniformity and the resistances at the contacts are considerably lower than that of the channel.

It is well known that metal-oxide surfaces are rich in defects, predominantly oxygen vacancies which serve as the binding sites for chemisorption processes. They also contribute to the scattering and trapping of charge carriers,[21] thus lowering the carrier mobility. To enhance device performance, it is crucial to passivate the surface states. As a result, we have employed CMOS compatible processes to passivate the surfaces of the nanowires with a SiO_2/Si_3N_4 bilayer coating patterned by a polyimide shadow mask. First, the untreated nanowire FETs were placed in a vacuum chamber (10^{-6} torr) to remove the surface adsorbents such as O_2 and H_2O, and then deposited with a layer of SiO_2 (100 nm) to prevent subsequent chemical readsorption. Afterwards, a layer of 50 nm Si_3N_4 was grown on top of the SiO_2 by plasma enhanced chemical vapor deposition (PECVD) under a temperature of 250 °C to cover the pinholes in the SiO_2 layer, as well as to improve the chemical resistance of the fabricated devices. Because the PECVD process is conducted at an elevated temperature, it produces an additional annealing effect that further optimizes the crystallinity of the SiO_2 coating, and it also improves the contact between the ZnO nanowire and the Ti/Au electrode, yielding a low resistive Ohmic contact.[19]

To distinguish the changes contributed by the surface passivation, two groups of devices have been prepared: 20 untreated FET devices with nanowire channel exposed to the air and 20 surface treated devices coated with SiO_2/Si_3N_4 passivation layers. For a representative sample without any surface treatment, the source-drain current versus gate voltage (I_{DS}-V_{GS}) curves are shown in Fig. 4(a). The Q1D carrier concentration and field effect mobility are estimated to be 4.0×10^7 cm^{-1} and 30 cm^2/V s using a simple electrostatic model based on a cylindrical wire with diameter of ~80 nm and length of ~4 μm.[1,5,22] The subthreshold swing $S \equiv \log[dV_{GS}/d(\log I_{DS})]$, a key parameter for FET scaling, is about 3 V/decade.[23] On average, the 20 untreated devices show an on/off ratio of $\sim10^3$ (at V_{DS}=0.5 V) and mobilities ranging from 20 to 80 cm^2/V s, which are consistent with the previously reported values for ZnO nanowire FETs.[4,5,12,24] In comparison, another 20 devices were coated with passivation layer and depicted in Fig. 4(b). After the surface treatments, the I_{DS}-V_{GS} curves of a typical sample measured at different bias voltages (V_{DS}) are displayed in Fig. 4(c). They exhibit a clear saturation region and a significantly enhanced on/off ratio on the order of 10^4 (even at V_{DS}=5 mV). For this illustrated example with diameter of ~90 nm, a Q1D carrier concentration of 7.5×10^7 cm^{-1} and a much higher mobility of 3118 cm^2/V s are obtained. In addition, sub-threshold swing is reduced [Fig. 4(d)], yielding $S\sim150$ mV per decade. Statistically, the 20 surface-coated devices display mobilities ranging from 1200 to 4120 cm^2/Vs. The origin of the superior FET performance is attributed to two factors: (1) passivation of surface defect states, which act as scattering and trapping centers, and (2) reduction of surface chemisorption processes at oxygen vacancy sites. Conclusively, the SiO_2/Si_3N_4 passivation processes have proven to significantly enhance device performance in the subthreshold swing, on/off ratio, and mobility. On average, the field effect mobility of ZnO nanowire

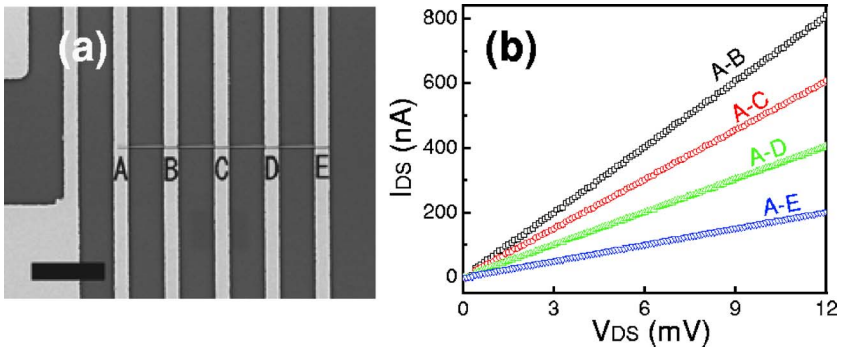

FIG. 3. (Color online) (a) SEM image displays the configuration of a nanowire device contacted with five electrodes, labeled as A–E (scale bar is 10 μm). (b) I_{DS}-V_{DS} characteristics of a ZnO nanowire measured across subsequent electrode pairs.

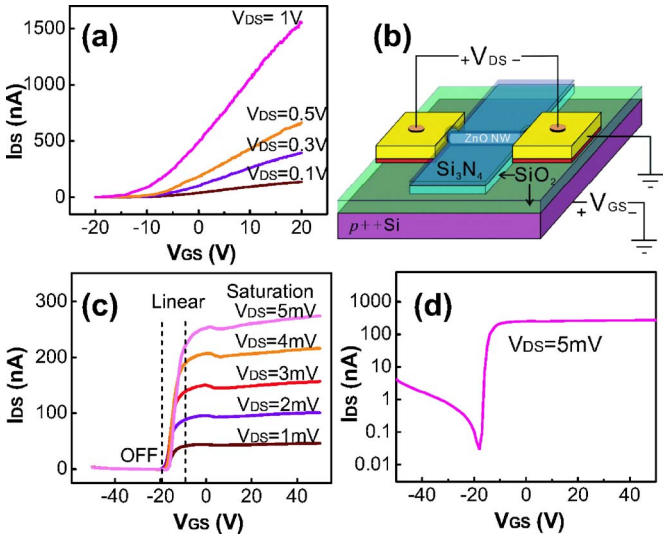

FIG. 4. (Color online) Transport measurements present (a) I_{DS}-V_{GS} curves of a ZnO nanowire FET without surface treatments showing typical *n*-type semiconducting behavior. (b) Schematic of surface passivated ZnO nanowire FET with SiO_2/Si_3N_4 bilayer covering the nanowire channel. (c) I_{DS}-V_{GS} of a surface treated nanowire FET exhibits significantly enhanced on/off ratio and transconductance. (d) Semilog plot demonstrates a tenfold reduction in the subthreshold swing. At large negative gate voltages, band bending gives rise to hole conduction.

FETs is dramatically increased by two orders of magnitudes, with the maximum measured mobility exceeding 4000 cm^2/V s. It is much higher than the reported mobility of Si nanowire FET (Ref. 2) (1350 cm^2/V s) and polymer coated ZnO nanorod FET (1200 cm^2/V s).[4]

In summary, we have presented remarkable device characteristics of field effect transistors based on ZnO nanowires synthesized by catalytic CVD method. The structural and PL analyses demonstrate the strong effect of the surface defect states. With a series of CMOS compatible surface passivations, the nanowire FETs exhibit improvement in the subthreshold swing, on/off ratio, and mobility. Since mobility determines the carrier velocity and thus switching speed, these nanowire FETs demonstrate promising potential as the building blocks for future applications in high frequency integrated electronics, such as memory element and logic gate.

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