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Electrically Dynamic Configurable WSe_2 Transistor and the Applications in Photodetector

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Non-destructive and reversible modulations of polarity and carrier concentration in transistors are essential for complementary devices. The fabricated multi-gated WSe_2 devices obtain dynamic electrostatic field induced electrically configurable functions and demonstrate as diode with high rectification ratio of 4.1×10^5, as well as n- and p-type inverter with voltage gain of 19.9 and 12.1, respectively. Benefiting from the continuous band alignment induced modulation of channel underneath the dual gates, the devices exhibit high-performance photodetection in wide spectral range. The devices yield high photo-responsivity (5.16 A W^{-1}) and large I_{light}/I_{dark} ratio (1×10^5). Besides, the local gate fields accelerate the separation of photo-induced carriers, leading to fast response without persistent current. This strategy takes the advantage of the simplified design and continues to deliver integrated circuits with high density. The superior electrical and photodetection characteristics exhibit great potency in the domain of future optoelectronics.

1. Introduction

Dimensional scaling of silicon-based transistors eventually approaches fundamental limits, accompanying with the issues of electrostatics, excessive leakage, and mobility degradations.[1,2] The ultrathin body as well as atomically flat surface of 2D semiconductors enables suppressing the short-channel effects, which helps in maintaining superior transistor performance down to extremely short channel lengths around 1 nm.[3–6] Complementary circuits have been widely implanted in advanced circuits for logic applications.[7–10] However, traditional doping strategies involve high-energy ion implantation or high-temperature diffusion,[11] and thus introduce defects in in-panel lattice, leading to performance degradation, long-term stability and/or reliability issues, as well as low doping efficiency.[12,13] Therefore, they are not suitable for the ultrathin 2D materials. To avoid the damage imparted to the 2D lattice, previous reports mainly focus on utilizing the advantage of inherent polarity of different channel materials to realize complementary electronics for low power consumption.[14,15] Although some feasible synthesis methods are proposed to control the majority carrier type, the carrier mobility is below the theoretical limit.[16–19] Therefore, it is a challenge to tune the polarity of 2D transistors while maintaining intrinsic high performance.

Recently, electrostatic doping which would not rely on any destructive doping method has aroused great interest in this regard.[20,21] Many strategies of electrostatic doping such as floating gate modulation, ferroelectric gate, and multiple metal gate modulation have been noticed.[22–24] Multiple gate electrodes have been utilized to modulate the polarity of transistors in 2D materials, such as MoS_2 and WSe_2.[25,26] However, most of the previous studies have employed the buried gate process, whereas the top gate process for multi-gate modulation has been rarely reported.[27] Moreover, most of the reported research focus on the electrical performance modulation of devices, and the photodetection performance is less studied.[27,28] In view of the unique properties of 2D materials, it has unique advantages in the construction of photodetectors.[29,30] For wide-spectrum photodetectors, it is essential to continuously modulate the band structure and obtain effective detection of specific incident light.[31–33] Therefore, it is necessary to conduct research on continuous modulation of band alignment for photodetectors.

In this work, electrically dynamic and configurable WSe_2 transistors are fabricated by using two top gates that define the polarity of channel regions. By tuning the two individual gate voltages, the polarity of the WSe_2 channel can be locally modulated, and thus n-type and p-type WSe_2 local regions are realized in an individual flake. And, the constructed n-type and p-type inverter

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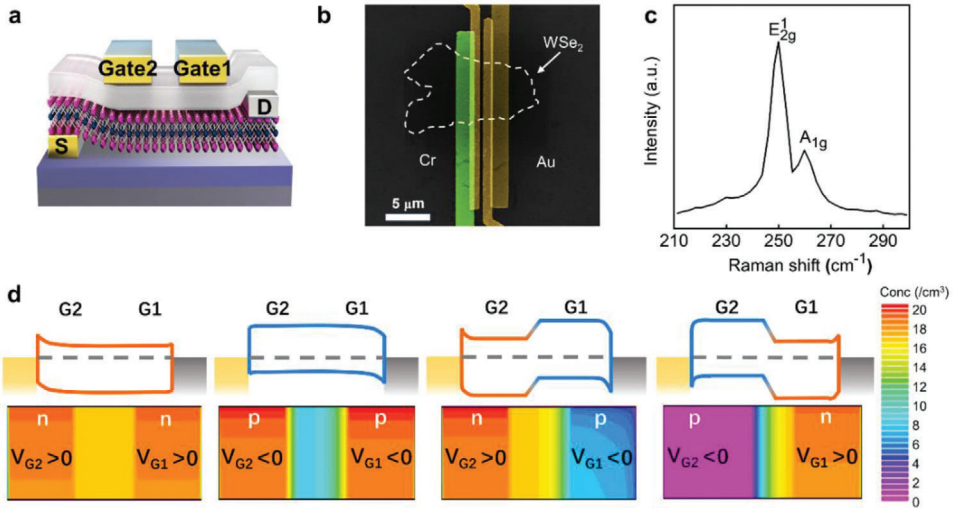


Figure 1. Device configuration and operation principles. a) Schematic image of the DTG WSe_2 transistor. b) Corresponding SEM image with 5 μm scale bar. c) Raman spectra of the WSe_2 channel. d) Band diagrams (upper panel) and simulation results of carrier distribution (lower panel) in WSe_2 channel with different gate voltages configurations. The gradient indicates the majority carrier distribution in the channel.

present high voltage gain of 19.9 and 12.1. Based on the continuous tuning of the band alignment in homogeneous channel and the use of asymmetric metal contacts, the device evolves from n–n, p–p to n–p, p–n diodes, which present superior ideal factors and high rectification ratio.[34–36] Moreover, by properly modulating the barrier height to construct p-type/intrinsic/n-type (p–i–n) homojunction, the devices can realize self-driven wide-band photodetection ranging from visible light to near-infrared ran with a high light/dark current ratio (I_{light}/I_{dark}) of 1×10^5, and fast response and recovery time of 553 and 604 μs, as well a highly efficacious photovoltaic energy conversion with output electrical power up to 3.57 nW μm^{-1}. Therefore, these electrically configurable transistors ease the assembling difficulty, and open up an avenue for future electronics and optoelectronics.

2. Results and Discussions

Figure 1a depicts the schematic diagram of the dual-top-gated (DTG) WSe_2 transistor. Figure S1, Supporting Information, schematically illustrates the device fabrication processes. Figure 1b is the scanning electron microscopy (SEM) image of electrically dynamic configurable WSe_2 transistor with top split-gate (about 250 nm apart) structure. Briefly, the source and drain electrode adopted asymmetric metal contact of Au and Cr, respectively. Few-layered WSe_2 flake with thickness of ≈4 nm (Figure S2, Supporting Information) is transferred as the channel. In this case, Van der Waals contacts are formed between WSe_2 channel and metal electrodes, and the metal-deposition–induced interfacial disorder is avoided, so that Schottky barrier is obtained.[37] Corresponding Raman spectra is shown in Figure 1c. By using atomic layer deposition (ALD), Al_2O_3 top-gated dielectric layer with a thickness of 10 nm is deposited. Subsequently, dual-gated configuration is completed by electron-beam lithography (EBL), metal deposition, and lift-off processes, which can realize electrostatic doping of the underneath WSe_2 channel.[38] As electric field can efficiently tune the band structure of WSe_2, the applied gate potential on the dual gates determine the doping profiles in the underneath WSe_2 channel, and efficaciously modulate the carrier injection from the contact metal. The upper panel of Figure 1d schematically illustrates the operation principles of four different band diagrams for varying polarity combinations with different gate voltages. In the DTG WSe_2 transistor, the gate at the drain side (gate1, G1) is used as a control gate, while the gate at the source side (gate2, G2) is used to program the device either to n- or p-type configuration. Various band alignments can be realized in an individual WSe_2 channel at different gate biases.[39] To design general polymorphic circuitry, this all-in-one device can be regarded as a basic unit. By dynamically configuring the applied gate voltages, selected digital switches with desired polarities are obtained. Electrical transfer characteristics with corresponding simulation results of charge major carrier distribution are shown in the lower panel of Figure 1d, which are performed by Silvaco technology computer-aided design based on the drift-diffusion model. The finite element approach is used to solve self-consistently the continuity equations and Poisson's equation for holes and electrons. Applied gate voltages create desired electrostatic doping in the underneath WSe_2 channel. When both V_{G1} and V_{G2} are biased positively, the conduction and valence bands bend downward and concentrate electrons in the channel. Due to the thinner Schottky barrier, the injection of electrons at Cr terminal is easier than that at Au terminal, resulting in n-type rectification behavior.[40] Conversely, negative voltages of V_{G1} and V_{G2} lead to the valence and conduction bands bending upward and gathering of holes in the channel. The injection of holes through the Au terminal is easier than that at the Cr terminal, culminating in a p-type rectifying behavior. When V_{G1} is negative and V_{G2} is positive, in this mode, holes are induced underneath G1 while electrons accumulate underneath G2. The device is conductive for the aforementioned three operation modes under positive V_{DS}. But when $V_{G1} > 0$ and $V_{G2} < 0$, the device transforms into off-current state, because of the built-in potential induced depletion region in the reverse-biased p–n junction. Therefore, altering the DTG potentials enables independent electrostatic control of carrier density in the WSe_2 channel and avoids dopant-related

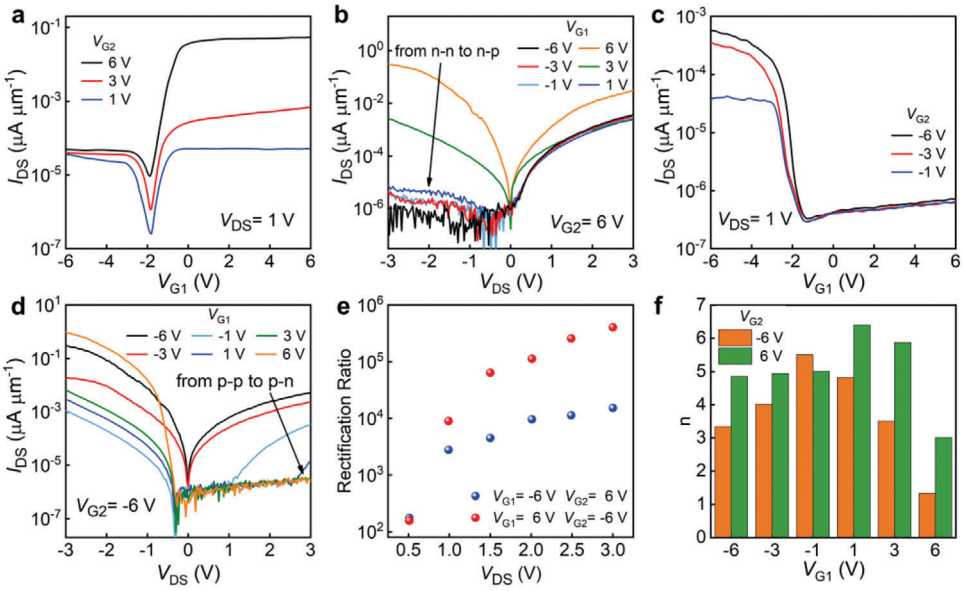
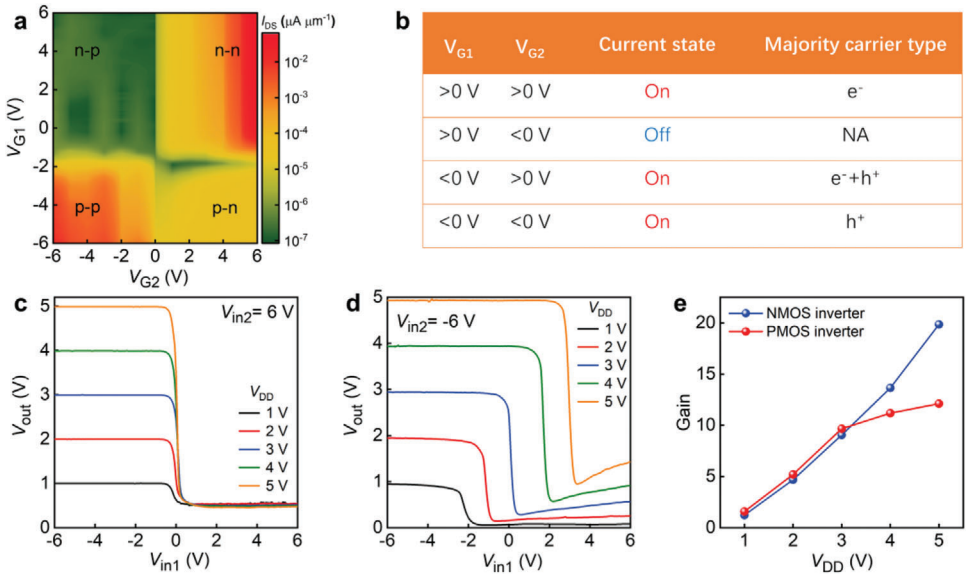


Figure 2. Electrical performance of the DTG device. a) Transfer characteristics of dual-gate asymmetric metal contact WSe_2 transistor. The positive V_{G2} programmed n-type configuration. b) Output characteristics at $V_{G2} = 6$ V. c) Transfer characteristics of negative V_{G2} programmed p-type configuration. d) Output characteristics at $V_{G2} = -6$ V. e) Extracted currents rectification ratio as a function of V_{DS}. f) Extracted diode ideality factor n with different V_{G1} under $V_{G2} = -6$ V and $V_{G2} = 6$ V.

issues, thus allowing access to various electronic configurations with different device operation modes.

To confirm that the gate bias can readily modulate the polarity and current of WSe_2 channel, a top-gated transistor operation is performed in Figure S3a, Supporting Information, which presents typical ambipolar transfer characteristic of WSe_2 transistors with symmetric Cr/Au contacts. The Fermi level pinning effect induces slightly lower barrier heights for electron injection, leading to the higher current of the n-type region.[41] And, the corresponding output curves also exhibit obvious rectifying behavior, as is shown in Figure S3b, Supporting Information. Based on the efficient n-type and p-type doping by gate biases, to achieve polymorphic operations with an individual WSe_2 flake, we design a DTG architecture to reconfigure doping profiles of the channel via electrostatic gating. Figure S4a, Supporting Information, shows the leakage current I_{GS} with different V_{G1} and V_{G2}, and I_{GS} is lower than 1 pA μm^{-1}. With the positive V_{G2}, the channel is doped electrostatically into n-type in which the electrons act as the majority carriers (**Figure 2**a). Corresponding output characteristics are shown in Figure 2b. When V_{G2} is fixed to 6 V, the channel underneath V_{G2} is electrostatically doped to be n-type. In this case, by decreasing V_{G1} from 6 to −6 V, the channel changes from n–n state to n–p state. The channel also can be programed into p-type when V_{G2} is negative in which the holes act as the majority carriers (Figure 2c). Figure 2d shows corresponding output characteristics. By fixing $V_{G2} = -6$ V, holes are accumulated in the channel underneath. When V_{G1} increases from −6 to 6 V, the height of Schottky barrier between WSe_2 and Cr is lowered, and then the channel changes from p–p state to p–n state. Because of the large barrier between Au and WSe_2 and a negligible barrier between Cr and WSe_2, Schottky junction is formed, which further suppresses the reverse current and significantly promotes the rectification ratio. Figure 2e reveals the gate-dependent rectification ratio as a function of V_{DS}. The rectification ratio increases with V_{DS}, and reaches peak values of 1.5×10^4 ($V_{G1} = -6$ V, $V_{G2} = 6$ V) and 4.1×10^5 ($V_{G1} = 6$ V, $V_{G2} = -6$ V) at $V_{DS} = 3$ V, respectively. Figure 2f extracts the ideality factor (n) of the obtained diode with different V_{G1} as $V_{G2} = -6$ V and $V_{G2} = 6$ V, respectively, which demonstrates a low value of 1.33. And thus, the excellent diode characteristics demonstrate electrically dynamic configurable diodes have few defects. Based on the efficient electrostatic doping of WSe_2 channel, the transportation characteristic can be readily modulated, which presents an evolution from rectifying state to non-rectifying state, and the conduction direction can be tuned as well (Figure S4b,c, Supporting Information).

By modulating the voltage configurations of the dual gates, the polarity and transport behaviors can be readily tuned, and virtual n-/p-type regions in the WSe_2 channel enables multiple operating modes by implementing the DTG gate configuration. We define V_{G1} and V_{G2} as input signals and I_{DS} as the output signal, the I_{DS} at $V_{DS} = 1$ V as a function of V_{G1} and V_{G2} are shown in **Figure 3**a. Based on the electrically dynamic configurable doping profile of the WSe_2 channel underneath G1 and G2, Figure 3b lists four current states available in the DTG device, which presents a variety of operation behaviors beyond traditional transistors.[42–45] To realize the configurable multifunctional logic application, we fabricate logic inverters based on the dynamic configurable WSe_2 transistor, and the basic logic applications are realized by controlling the polarity and magnitude of V_{G1} and V_{G2}. In both of n-type and p-type inverters, direct-coupled field-effect transistor logic technology is used, as shown in Figure S5a, Supporting Information, and G2 (V_{in2}) is defined as the polarity control terminal. To obtain high transconductance and output current, the contact region is fully overlapped by the gate region. We insert a saturated transistor between the power supply



V_{G1}	V_{G2}	Current state	Majority carrier type
>0 V	>0 V	On	e^-
>0 V	<0 V	Off	NA
<0 V	>0 V	On	e^-+h^+
<0 V	<0 V	On	h^+

Figure 3. Configurable logic functions. a) I_{DS} is mapped as a function of V_{G1} and V_{G2} with V_{DS} = 1 V. b) Current states and majority carrier types with different applied gate voltages (V_{G1} and V_{G2}). c) Voltage transfer characteristics of n-type inverter. d) Voltage transfer characteristics of p-type inverter. e) Extracted voltage gain as a function of V_{DD} for n-type and p-type inverters, respectively.

(V_{DD}) and n-type inverter. For p-type inverter, the saturated transistor is inserted between the inverter and grounding terminal (GND). Figure 3c,d exhibits the voltage transfer characteristics of n-type and p-type inverters with different supply voltages of G1 (V_{in1}) and V_{DD}. By applying V_{G2}, as shown in Figure 3c, the n-type inverter exhibits typical transfer curves by fixing V_{in2} = 6 V. Figure S5b,c, Supporting Information, shows the corresponding voltage gain of n-type and p-type inverters with different V_{DD}. For p-type inverter (Figure 3d), by fixing V_{in2} = −6 V, the device exhibits steep transformation of output voltage versus input signal. Figure 3e plots the extracted maximum voltage gain with different V_{DD} of n-type and p-type inverters, and peak values of 19.9 and 12.1 are obtained at V_{DD} = 5 V, respectively. Therefore, DTG device shows promising applications in building more simplified and advanced logic circuits.

As the band alignment in the WSe_2 channel is readily tuned by the electrostatic field, the barrier can be continuously modulated as well, and thus photodetectors that are sensitive to specific wavelengths are designed. **Figure 4**a shows typical output curves with 532 nm laser illumination at V_{G1} = 6 V and V_{G2} = −6 V. The gate electrostatic fields can create different polarities region in WSe_2 channel, and due to a 250 nm gap between G1 and G2, a p–i–n junction is constructed. In this configuration, the spontaneously photo-induced carriers can be efficiently accelerated and separated.[46] A high I_{light}/I_{dark} ratio of around 1×10^5 is obtained at a power intensity P_{light} = 50 mW cm^{-2}. Under forward drain–source voltage (V_{DS} = 3 V), the responsivity (R) and I_{light}/I_{dark} values are strongly correlated by the incident laser power (P_{light}) (Figure 4b and Figure S6, Supporting Information). With the increment of P_{light}, photo-induced carrier recombination is enhanced, and R is decreased.[47] The highest R at P_{light} = 0.038 mW cm^{-2} is 5.16 A W^{-1}, which is much higher than that of typical WSe_2-based photodiodes (≈0.17 A W^{-1}).[48] Figure 4c shows the on–off switching characteristics under multiple test cycles of the DTG device under 532 nm laser illumination with P_{light} = 50 mW cm^{-2}, demonstrating fast and reliable on–off switching performance. In electrostatic field modulated photodiode, the intrinsic region significantly reduced the junction capacitance and I_{dark}.[49] As a result, the response and recovery speed of the device are much faster than traditional heterostructure devices.[50] As shown in Figure 4d, the response time (τ_{rise}) and recovery time (τ_{decay}) are defined as the time width of the peak photocurrent to rise from 10% to 90% and fall from 90% to 10%, which are recorded to be 533 and 604 μs, respectively. The p–i–n photodiode can also apply to harvest photovoltaic energy. As shown in Figure S7a, Supporting Information, the open circuit voltage (V_{OC}) is relatively low at the weak light intensity, probably due to the recombination of photo-induced carriers.[47] Moreover, high incident light intensity promote high photo-induced carriers concentration, leading to the increment of V_{OC} value. According to the V_{OC} and I_{SC} extracted from Figure S7a, Supporting Information, the power generated in the electrostatic field modulated photodiode is plotted in Figure S7b, Supporting Information. The output electrical power increases with P_{light} and obtains a peak value of 3.57 nW μm^{-1} at P_{light} = 50 mW cm^{-2}. The I_{SC} is also affected by V_{G1} and V_{G2}. As shown in Figure 4e, by fixing V_{G2} = −5 V, the I_{SC} increases with V_{G1} when P_{light} = 10 mW cm^{-2}. With fixed positive V_{G1} and negative V_{G2}, the channel underneath G1 is electrostatically doped p-type and n-type regions enable efficient separation of photo-induced carriers, leading to increased I_{SC}. Besides, the larger voltage difference applied between two top gates, the faster response, and recovery time could be realized (Figure S8, Supporting Information). As the barrier height between WSe_2 channel underneath G1 and G2 can be continuously modulated, the detection region can be expanded by adjusting the gate potentials. Figure S9, Supporting Information, shows the output plots at V_{G1} = 6 V, V_{G2} = −6 V under different incident light illumination. Notably, the laser power intensity is fixed at

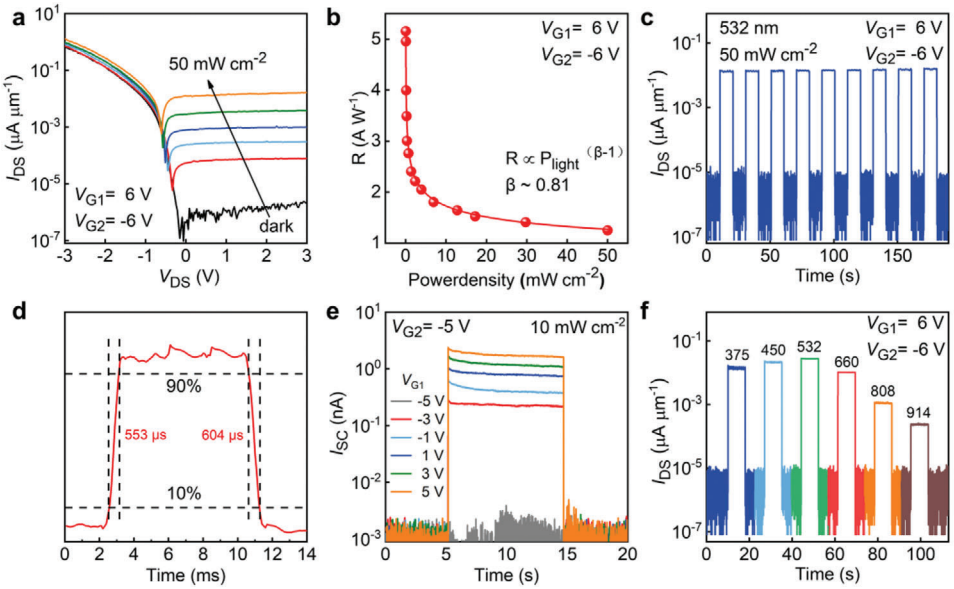


Figure 4. Gate voltage and laser power dependent photoresponse. a) I_{DS}–V_{DS} characteristics of DTG device under 532 nm laser illumination with different power intensity. b) Extracted photoresponsivity as a function of incident power at V_{G1} = 6 V and V_{G2} = −6 V. c) Time-dependent dynamic photoresponse under light illumination with a power intensity of 50 mW cm^{-2}. d) Corresponding response time (τ_{rise}) and recovery time (τ_{decay}) of the obtained photodetector. e) Short-circuit current I_{SC} under 532 nm incident light illumination with different V_{G1}. f) Typical photoresponse performance of the device under incident light illumination with different wavelengths.

20 mW cm^{-2} for all measurements. Figure 4f demonstrates that the near-infrared light detection can be achieved with effective electrostatic doping. The photocurrent decreases obviously for the wavelengths beyond 660 nm, which is probably due to the reduced photon energy at long wavelength.[51] Therefore, the strategy presented here is sufficient to construct high-performance photodetectors that are sensitive to specific incident light illuminations, by modulating the electrostatic doping levels of the gate.

3. Conclusion

In summary, electrically dynamic configurable WSe_2 transistors are fabricated, and various device operation modes are realized by tuning the local electrostatically doped channel profile. With different gate bias and circuit configurations, high voltage gain is obtained. By using asymmetric metal contacts, hole and electron injections are promoted, and the devices present desirable rectification ratio. The continuous modulation of barrier height enables multi-color photodetection with high responsivity. The built-in electric field of the p–i–n junction and the Schottky barriers at the contact region spontaneously separates the photo-induced carriers for fast and transient recovery. The obtained highly effective photovoltaic energy conversion is also suitable for self-driven broadband photodetection. Therefore, the present strategy provides great potential for the development of multi-functional optoelectronic devices.

4. Experimental Section

Device Fabrication: EBL was used to pattern the source electrode. Metal thermal evaporation and lift-off approach were used to fabricate 50 nm Au source electrode with an extended contact on SiO_2 (300 nm)/Si substrate. Next, a few-layered WSe_2 flake was transferred by PDMS stamp as channel. The thickness of WSe_2 flake was ≈4 nm as confirmed by atomic force microscopy. Cr (50 nm) drain electrode was patterned on WSe_2 flake using EBL and metal thermal evaporation. 10 nm Al_2O_3 dielectric layer was deposited by ALD, and Cr/Au (10/50 nm) dual-gate electrodes were formed above Al_2O_3 dielectric layer by EBL and thermal evaporation.

Material Characterization and Device Measurement: The morphology of the homojunction was characterized by scanning electron microscope (JEOL IT300) and atomic force microscope (Park NX20). Raman spectra were characterized on Renishaw Raman spectrometer platform. Agilent 4156B semiconductor parameter analyzer and Lakeshore TTPX probe station were used to measure the electric and photoelectric characteristics. The light sources were lasers with wavelengths of 375, 457, 532, 660, 808, and 914 nm, respectively.

Device Simulations: Device simulations were performed using Silvaco-TCAD. The model used in the software was based on the drift-diffusion method, where Poisson's equation and continuity equations for electrons and holes were solved self-consistently by the finite element approach. In order to present the electron density distribution in the cross-section of the device more clearly, the thickness of the WSe_2 flake was set at 4 nm and the channel length was set at 2 μm during the simulation. The models used in the simulation included conmob, auger, and srh. The Newton iteration method was used for the calculation.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

electrostatic doping, inverters, photodetectors, WSe_2

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