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High Mobility MoS_2 Transistor with Low Schottky Barrier Contact by Using Atomic Thick h-BN as a Tunneling Layer

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Graphene has been studied for a long time since it was first discovered in 2004.[1,2] However, the lack of band gap limits its application for logic devices.[3] In recent years, transitional metal dichalcogenides, such as MoS_2, have triggered intensive interests for their unique characteristics such as wide band gap (1.8 eV for monolayer and 1.2 eV for multilayers) and high mobility.[4–10] In addition, the dangling-bond-free surface and the atomic thickness can reduce the short channel effect thus making it a promising candidate for short channel devices.[3] The field effect transistors (FETs) based on MoS_2 can demonstrate high on/off ratio of 10^8 and near perfect subthreshold swing values of 65 mV dec^{-1}.[11] Although the phonon limited mobility of MoS_2 on SiO_2 can be as high as 410 cm^2 V^{-1} s^{-1}, most reported field effect mobilities (μ_{FE}) under room temperature are still much lower than this value.[12] Contact resistance is one of the key factors attributing to the loss of mobility since the formation of a Schottky barrier for electron injection greatly limits the FETs performance.[13] A number of past works have been conducted to improve the contact resistance recently.[6,14–24] For example, phase engineered MoS_2 can greatly reduce the contact resistance while the metastable 1T phase MoS_2 limits its application.[25] On the other hand, the chloride doping method can also improve electron doping level and reduce the contact resistance, nevertheless this method significantly shifts the threshold voltage and can only dope the entire MoS_2 flake.[21,26] Additionally, graphene could be also used as electrode to achieve low contact resistance due to the gate tunable Fermi level.[27,28] Unfortunately, this method relies on exfoliated graphene, which is not scalable and difficult to control, thus it is not applicable for large scale fabrications. Recently, a new approach to reduce the contact resistance is to insert an ultrathin tunneling layer into the contact interface to form a metal–insulator–semiconductor (MIS) structure.[15,29] For example, Lee et al. reported that Schottky barrier height of MoS_2-metal contact can be reduced to 29 meV with 1.5 nm Ta_2O_5 tunneling layer on chemical vapor deposition (CVD) MoS_2. However, direct atomic layer deposition on the dangling-bond-free MoS_2 surface usually results in large isolated islands and thus it is not suitable for application on the perfect 2D materials.[11,30]

In this work, CVD hexagonal boron nitride (h-BN) tunneling layer was used to reduce the Schottky barrier height and improve the contact between metal and MoS_2. Benefiting from the atomic thickness of 1–2 layers h-BN, the Schottky barrier can be greatly reduced with small tunneling resistance. After inserting an ultrathin layer h-BN into to the contact interface, we obtained the reduced Schottky barrier height of 31 meV and contact resistance of 1.8 kΩ·μm, which were improved from 158 meV and 5.1 kΩ·μm, respectively. It was observed that further increasing the thickness of h-BN did not significantly reduce the Schottky barrier height; however, it will increase the tunneling resistance. Owing to the optimized tunneling contact, a typical FET showed a high field effect mobility of 73.0 cm^2 V^{-1} s^{-1} and output current of 330 μA $μm^{-1}$ at room temperature, which can be further improved to 321.4 cm^2 V^{-1} s^{-1} and 572 μA $μm^{-1}$ at 77 K, respectively. Meanwhile, negative differential resistance (NDR) effect was also obeserved at low temperature, which can be attributed to self-heating effect, indicating the importance of heat dissipation. This work provided a deeper insight look for MIS contact and is a promising way to achieve low contact resistance on MoS_2 in large scale.

Here, a MoS_2 flake was mechanically exfoliated onto the SiO_2/Si (255 nm thick thermal oxide) substrate by the scotch tape method.[1,3] CVD h-BN was then transferred onto the substrate to cover the entire MoS_2 flake as shown in **Figure 1**a–c (Raman peak frequency of the h-BN is indexed in Figure S1, Supporting Information). Scanning electron microscope (SEM) image, optical image and side view schematic of the fabricated device are exhibited in Figure 1d. The thickness of the CVD grown h-BN was confirmed to be 1–2 layers by atomic force microscopy (AFM) measurement at the edge of the film as shown in Figure 1e. The thickness of these MoS_2 flakes was evaluated to be 4–5 layers by optical microscopy and Raman

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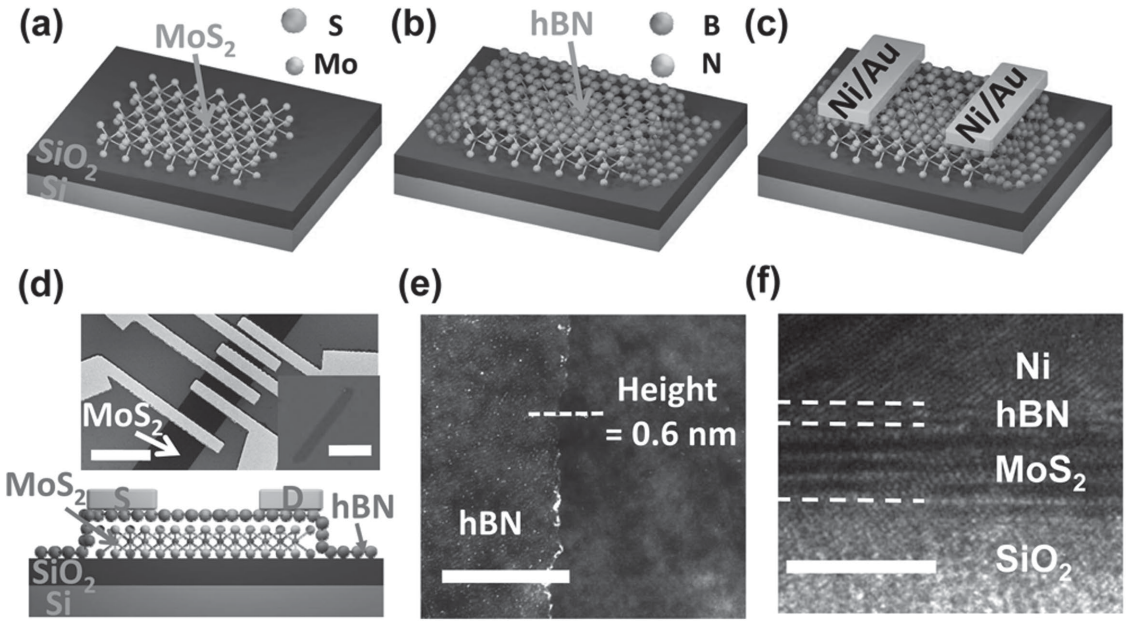

Figure 1. a–c) Fabrication process of the device. d) SEM image, optical image, and side view schematic of the fabricated device. The scale bar is 5 μm and channel lengths are 2, 1, 0.7, 0.5, and 0.3 μm, respectively. The scale bar in the optical image is 15 μm. e) AFM image at the edge of the film of the CVD grown h-BN. The thickness of the h-BN is 0.6 nm, indicating 1–2 layers h-BN. The scale bar is 2 μm. f) Cross-sectional HRTEM image of the interface between MoS_2 and h-BN. The scale bar is 5 nm.

spectroscopy since the Raman peak frequency difference between the A_{1g} peak and E^1_{2g} peak was found to be 24 cm^{-1} as shown in Figure S2 (Supporting Information).[11] The Raman peak frequency of the MoS_2 showed no shift after coverage with the h-BN layer (Figure S2, Supporting Information), indicating marginal damage or lattice distortion brought by h-BN.[11] The cross-sectional high-resolution transmission electron microscopic image of h-BN/MoS_2 stack is presented in Figure 1f which exhibits bi-layer h-BN and 4 layers MoS_2 with uniform interface. The arrays of devices with various channel lengths were defined via electron beam lithography (EBL) and subsequent metal deposition.

Figure 2a is the transfer characteristics of back gated MoS_2 FETs with and without h-BN tunneling layer contact (hysteresis is given in Figure S3, Supporting Information). As shown in Figure 2a, the threshold voltage shifted negatively with increase of work function of contact metal, which was consistent with previous reports about MoS_2 contacted by scandium.[14] After the coverage of CVD h-BN, the turn-on voltage showed a small negative shift compared with the MoS_2-metal contact, which was also observed in previous works on tunneling contact.[15] As the current is determined by both the channel and the contact for a Schottky contact transistor, the transistor becomes easier to be turned on when the contact resistance is reduced. The field effect mobility μ_{FE} is estimated using the equation

$$\mu = \left(\frac{L}{WC_{ox}}\right)\frac{g_m}{V_{ds}} \quad (1)$$

where L and W are the channel length and width, C_{ox} is the oxide capacitance of 13.6 nF cm^{-2}, $g_m = dI_{ds}/dV_{gs}$ is the transconductance and V_{ds} is the drain to source bias of 1 V. The peak field effect mobilities of the FETs with Ni, Au, and Pd metal contacts were 46.7, 36.4, and 26.2 $cm^2\ V^{-1}\ s^{-1}$, respectively (Figure 2b). However, with the h-BN interfacial contact layer, the mobilities became 73.0, 43.1, and 23.7 $cm^2\ V^{-1}\ s^{-1}$ for these three metals. Particularly, Ni/Au contact with h-BN tunneling layer showed the highest mobility of 73.0 $cm^2\ V^{-1}\ s^{-1}$. The I_{ds}–V_{ds} curves under different gate bias for the devices of Ni/Au and h-BN/Ni/Au contact are given in Figure 2c. The output curves showed good linear relationship at low V_{ds} while the device with h-BN tunneling layer showed much higher output current. It is known that for a metal contact, metal interacts with MoS_2 and results in high interface density of state near MoS_2 conduction band. The penetration of metal induced gap state (MIGS) results in the high Schottky barrier height for metal contact as shown in Figure 2d.[29] Inserting a h-BN layer does not alter the MoS_2 bands, indicating weakened interaction at the interface. The penetration of MIGS is reduced by using the atomic h-BN insulator, which results in a reduced Schottky barrier height (Figure 2e). Another mechanism is the electronic dipole formation at the insulator–semiconductor or metal–insulator interface (Figure 2f). The dipole at the h-BN/MoS_2 interface arises from misalignment of charge neutrality level between h-BN and MoS_2. The dipole at the metal/h-BN interface is formed as a result of charge transfer between metal Fermi level and the h-BN charge neutrality.[29,32] The interfacial dipoles of opposite polarity can neutralize charges at the interface and prevent the intrinsic Fermi level from moving toward the charge neutrality level thus reducing the Schottky barrier height. As for the traditional MIS structure, the dielectrics is usually set to be 1–3 nm to achieve a balance between Schottky barrier height and tunneling resistance.[29] For ultrathin CVD h-BN within 0.6 nm, the reduced insulator thickness makes electrons easier for direct tunneling.[22,29,32] Moreover, the CVD h-BN contains more defects than exfoliated h-BN, which also

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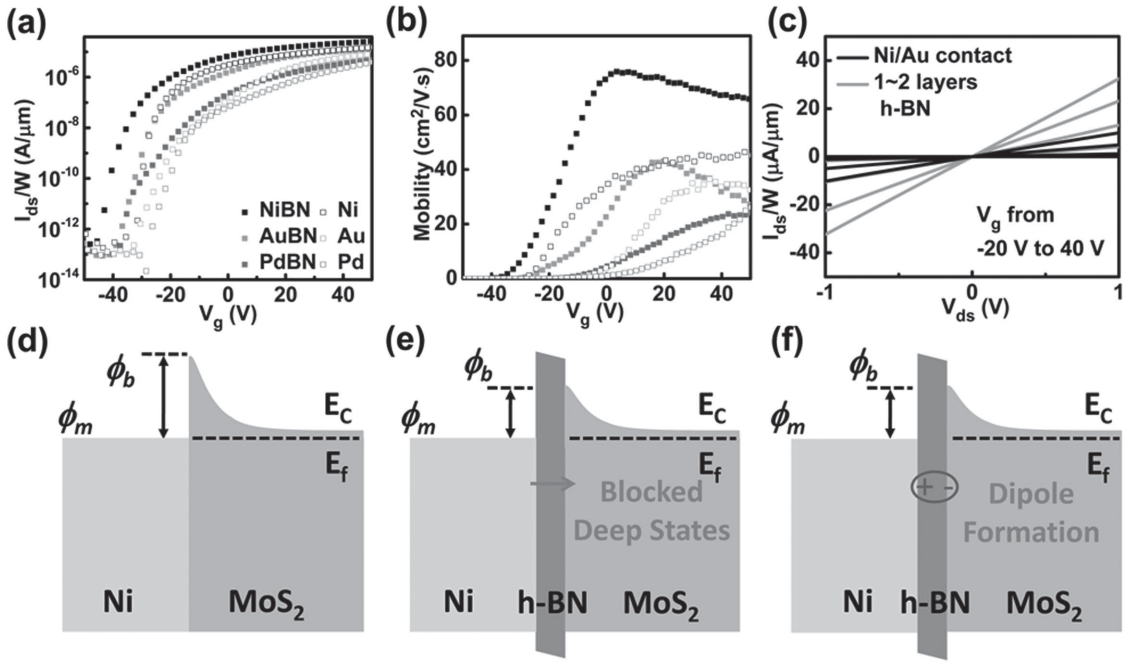

Figure 2. a) Transfer characteristics of FETs with Ni/Au, Au, and Pd/Ag contact. Solid dots are the FETs with metal contact and hollow dots are the FETs contact with CVD h-BN tunneling layer, channel length is 2 μm, V_{ds} = 1 V. The thicknesses for the devices given in this figure are 5 layers to reduce the variation caused by the MoS_2 thickness. b) Mobility against the back gate bias. c) I_{ds}–V_{ds} curves under different gate bias for the devices with/without h-BN. The output curves show good liner relationship at low V_{ds} with/without h-BN, but the one with h-BN tunneling layer shows much high output current. d) Simplified band diagram for Ni/Au contact, the barrier height is high as a result of penetration of MIGS. e) Simplified band diagram for h-BN/Ni/Au contact. The Schottky barrier is reduced while the tunneling resistance is small due to the atomic thickness of h-BN. The barrier height is reduced by minimizing the penetration of MIGS. f) The barrier is reduced as a result of dipole at the interface. The metal/h-BN dipole arises as a result of electronic charge transfer between the metal Fermi level and the h-BN charge neutrality level. The dipole at the van der Vaals heterointerfaces arises from charge neutrality level misalignment between the h-BN and MoS_2.

plays an important role in tunneling transport (Figure S4, Supporting Information).[31–33]

To further explore the Schottky barrier height of the contact, we mainly focus on the h-BN/Ni/Au contact since it showed the highest performance so far. For a Schottky barrier device, the current in the subthreshold region mainly depends on the thermionic emission current and the thermally assisted tunneling current.[14,20,22] According to the thermionic theory, when the back gate voltage is below flat-band voltage, the current can be written as

$$I_d = A^*_{2d} T^{3/2} \exp\left(\frac{q\phi_B}{k_B T}\right)\left[1-\exp\left(-\frac{qV_{ds}}{k_B T}\right)\right] \quad (2)$$

where A^*_{2d} is the 2D equivalent Richardson constant, I_d is the current through the device, T is the absolute temperature, k_B is the Boltzmann constant, q is the electronic charge and V_{ds} is the drain to source bias of 1 V.[6,20,22] When the back gate voltage (V_{GS}) is below flat-band voltage (V_{FB}), the thermionic emission current dominates the current. When V_{GS} is larger than V_{FB}, thermally assisted tunneling current becomes significant and adds on other component that is not included in the thermal emission theory, which results in the nonlinear behavior. When V_{GS} equals to the V_{FB}, Φ_B can be accurately extracted from the slope since thermally assisted tunneling does not contribute to the current. The value of $\ln(I_d/T^{3/2})$ at a fixed drain bias is given in **Figure 3**a–c and the slope of the line is the barrier height at various back gate bias. Figure 3d–f is the effective Schottky barrier height as a function of gate bias with different h-BN thickness. Obviously, metal contact showed the highest Schottky barrier height of 158 meV. After 1–2 layers h-BN insertion, the barrier height was reduced to 31 meV. Further increasing h-BN layer to 3–4 layers resulted in a similar barrier height of 38 meV, which showed no improvement compared with the thinner ones.

For a MIS structure, the contact resistance is mainly determined by the Schottky barrier and the tunneling resistance.[29,32] Inserting an insulating layer at the contact can reduce the Schottky barrier height but will increase the tunneling resistance. Thick insulating layer will result in large tunneling resistance and decrease the current flow through the device. In order to identify an optimized h-BN thickness, contact resistance with different h-BN thickness was measured using transfer length method as shown in Figure S5 (Supporting Information). **Figure 4**a–c shows contact resistance (R_c) and total resistance (R_{total}) versus gate voltage. It can be seen that both the contact resistance and the total resistance exhibited strongly dependence on the back gate bias. The device with 1–2 layers h-BN contact showed the smallest contact resistance of 1.8 kΩ·μm at a carrier density of $n = C_{ox}V_{gt} = 5.1 \times 10^{12}$ cm^{-2}, which was significantly lower than 5.1 kΩ·μm of the Ni/Au contact. This is due to the reduced Schottky barrier height as shown in Figure 3. In the case of

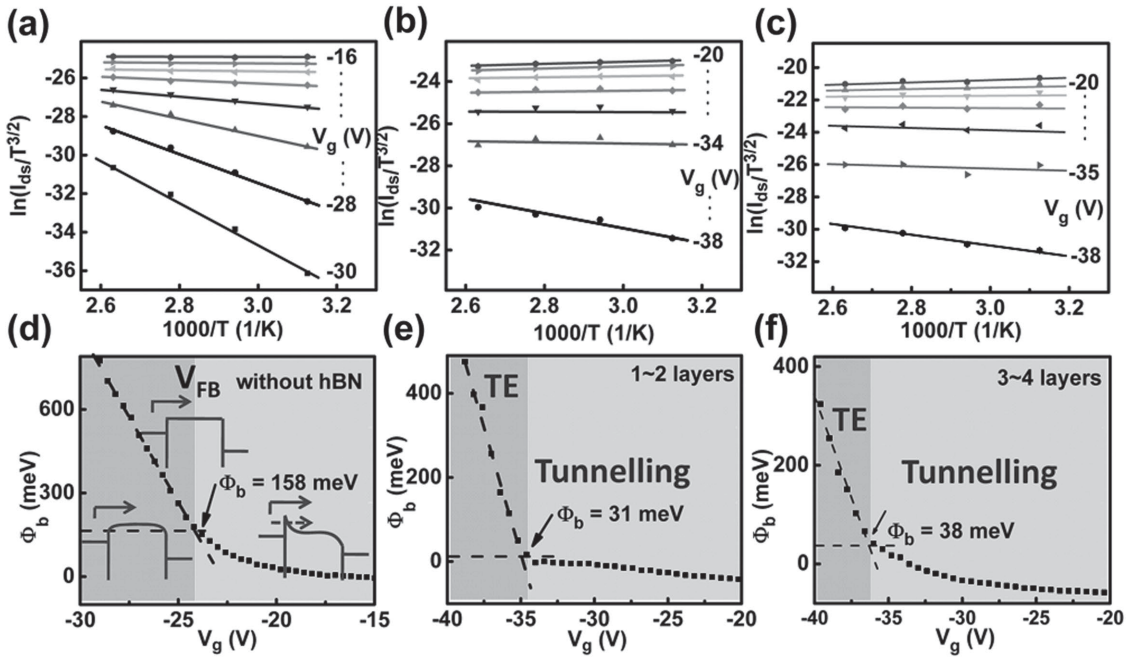

Figure 3. a–c) The Arrhenius plots for different back gate bias when thicknesses of h-BN are 0 layer a), 1–2 layers b), and 3–4 layers c), respectively. The slopes of the lines correspond to the Schottky barrier height for corresponding gate bias. d–f) The Schottky barrier heights for different back gate bias when thickness of h-BN are 0 layer d), 1–2 layers e), and 3–4 layers f), respectively.

metal contact, Schottky barrier dominates the contact resistance. Inserting an ultrathin h-BN tunneling layer can reduce the Schottky barrier height while the tunneling resistance is relative small due to the atomic thickness. However, the contact resistance for 3–4 layers h-BN was 3.2 kΩ·μm, which was larger than that with thinner h-BN. Since the Schottky barriers for them were similar as shown in Figure 3, the change in the contact resistance was probably caused by the increased tunneling resistance. For the relative thick h-BN, tunneling resistance plays a major role and dominates the contact resistance.

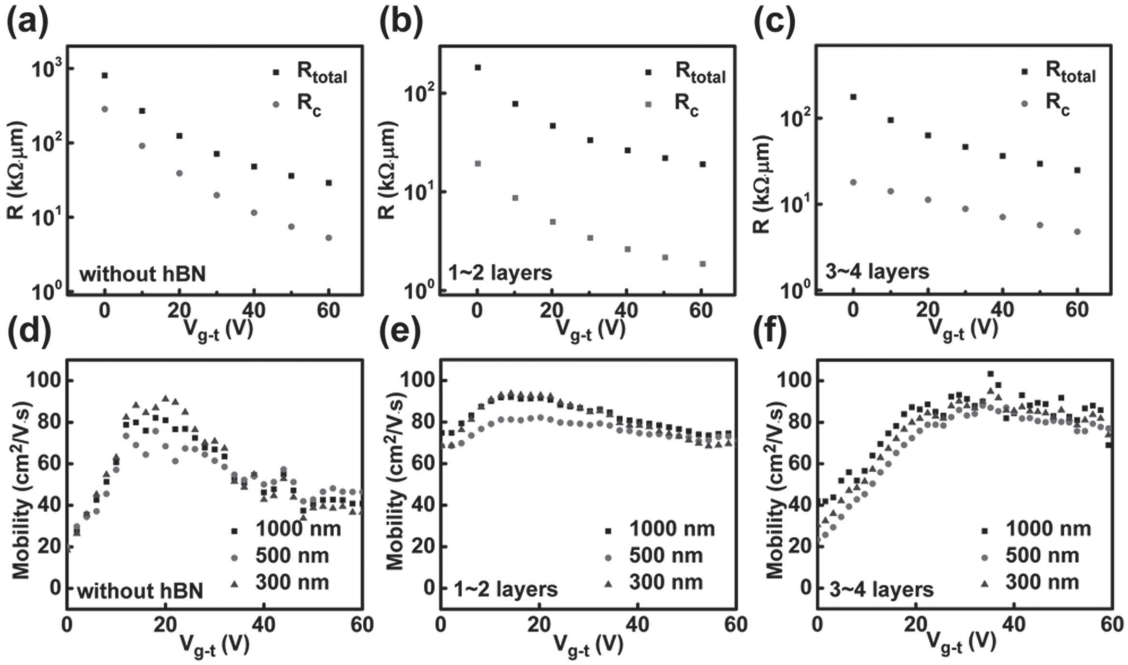

Figure 4. a–c) The total resistances and contact resistances for different back gate bias when thickness of h-BN are 0 layer a), 1–2 layers b), and 3–4 layers c), respectively. d–f) The field effect motilities as a function of the back gate bias with various channel length when thickness of h-BN are 0 layer d), 1–2 layers e), and 3–4 layers f), respectively.

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In this regard, 1–2 layers are the most suitable thickness of h-BN for this MIS contact structure.

It has been reported that the exfoliated h-BN can act as a encapsulate layer to reduce the scattering at the interface.[27] To investigate the influence of CVD h-BN to the channel, we carefully subtracted the R_c at different gate bias and the mobility without contact resistance could be calculated as

$$\mu = \left(\frac{L}{WC_{ox}}\right)\frac{d}{d(V_{bg}-V_{th})}\left(\frac{1}{R_{total}-2R_c}\right) \quad (3)$$

where L and W are the channel length and width, C_{ox} is the oxide capacitance, V_{bg} is the back gate voltage, V_{th} is the threshold voltage, R_{total} is the total resistance, and R_c is the contact resistance.[21] The effect of the contact resistance was subtracted using this method. Meanwhile, we can obtain the actual field effect mobility from the MoS_2 channel. As shown in Figure 4d–f, the peak field effect mobility of the MoS_2 channel was 90.7 $cm^2\ V^{-1}\ s^{-1}$, which was slightly higher than 73.0 $cm^2\ V^{-1}\ s^{-1}$ obtained directly with the transfer curve. After introducing a h-BN layer, the peak mobility without contact resistance increased a little. The h-BN act not only as a tunneling layer but also as an encapsulate layer to get rid of the influence of atmosphere and interfacial charge impurities scattering, thus can improve the channel conductance.[27,33] With 1–2 layers h-BN, the channel conductance without contact resistance is improved from 18.4 to 15.3 kΩ·μm. Benefiting from it, the mobility of the FET with h-BN showed little decrease at high V_{gs} region while the direct contact one showed strong mobility loss, which was consistent with previous report.[21] Considering the significant improvement in Figure 2, it can be confirmed that the improvement was attributed to the optimized contact resistance.

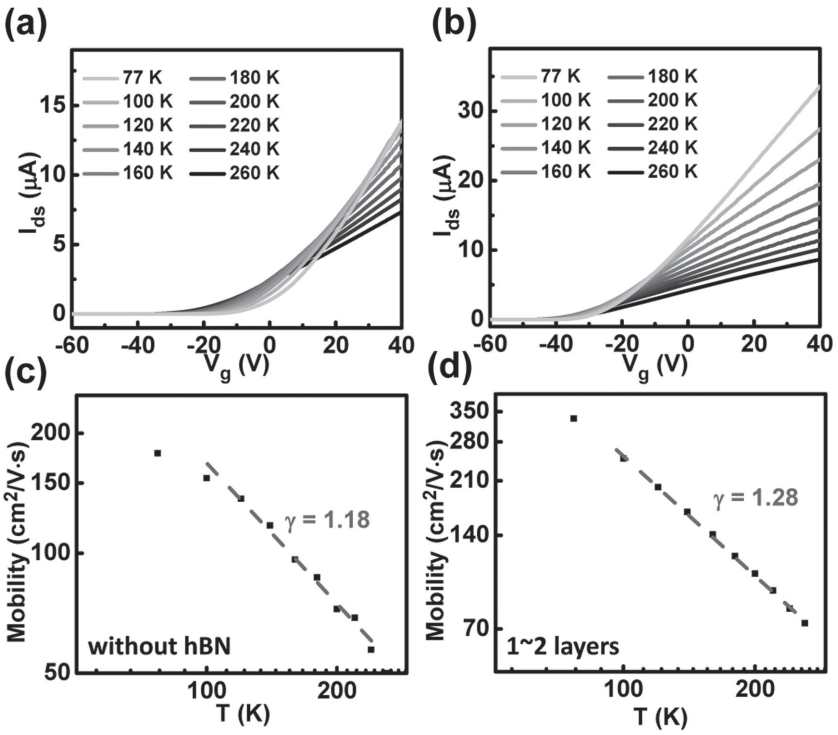

Figure 5. a,b) Transfer characteristics of FETs with metal contact a) and h-BN tunneling layer b), channel length = 2 μm, V_{ds} = 0.1 V. For Ni/Au contact, the conductivity decrease with increasing temperature when V_g > 30 V and increase with increasing temperature when V_g < 30 V. For h-BN/Ni/Au contact, the turning point decreased to −10 V. c,d) Temperature dependent mobility of FETs with metal contact c) and h-BN tunneling layer d). The exponent γ was 1.18 for Ni/Au contact and 1.28 for h-BN/Ni/Au contact.

Based on the optimized contact resistance, the characteristics of the devices were systematically examined at various temperatures considering the contact resistance shows less influence to the device performance. **Figure 5**a,b is the temperature dependent transfer characteristics of the devices with Ni/Au contact and h-BN/Ni/Au contact. For two terminal measurements, both the contact resistance and the channel resistance strongly influence the performance of the device. Generally the resistivity of MoS_2 channel decreases on cooling for the reduced phonon scattering.[28] On the contrary, the contact resistance increases on cooling according to the thermionic theory. At low bias, the contact resistance dominates the current. At higher gate bias, since other components that are not included in the thermal emission theory contribute to the current, the influence of the contact resistance becomes small. The conductivity will shows different temperature dependent behavior under different gate bias. For Ni/Au contact, the conductivity decreased with increasing temperature when V_g > 30 V and increased when V_g < 30 V. The metallic behavior turning point decreased to −10 V as to h-BN/Ni/Au contact, indicating small contact resistance. Since in the phonon limited region the mobility fits the expression $u \approx T^{-}\gamma$, the field effect mobility against the temperature is plotted in logarithmic scale as shown in Figure 5c,d.[12] As is shown in Figure 5c,d, power law dependence with a positive exponent is observed, indicating reduced phonon scattering at low temperature. The exponent γ was 1.18 for Ni/Au contact and 1.28 for h-BN/Ni/Au contact. These values were similar with the previous reports with graphene/MoS_2 contact.[27] In low temperature region, the current mainly depended on charge impurities and contact resistance.[27,28,34] Because of the relative high contact resistance for metal contact at low temperature, the mobility was 178.2 $cm^2\ V^{-1}\ s^{-1}$ at 77 K. For h-BN/Ni/Au contact, the mobility reached 321.4 $cm^2\ V^{-1}\ s^{-1}$, which was among the highest values compared with other contact methods without exfoliated h-BN encapsulate layer, indicating small Schottky barrier height.[20,24,27] The thick exfoliated h-BN encapsulate layers reduce the charge Coulomb scattering, which result in the higher mobility compared with our result at low temperature.[28]

To investigate the performance limitation of the device, output characteristics for device with 300 nm channel length on 100 nm SiO_2 was developed and then measured under different temperatures (The output characteristics are given in Figure S6, Supporting Information). The output current can reach 330 μA μm^{-1} at room temperature as shown in Figure S6a

(Supporting Information). When the temperature decreased to 77 K, the output current can reach 572 μA μm^{-1} as shown in Figure S6b (Supporting Information). When the current was above 500 μA μm^{-1}, NDR effect was observed, which was seen in the chloride doped device in previous report.[26] Due to the high output current, self-heating effect is not negligible since both the SiO_2 and the MoS_2 have low thermal conductivity. Using pulsed-IV method can help to reveal the impact of the NDR effect. In order to reduce the self-heating effect, pulse measurement was carried out with pulse width from 500 μs to 1 ms (Figure S6c, Supporting Information) and the $\Delta I/I_{sat}$ was given in Figure S6d (Supporting Information). The NDR effect was weakened during the on state with short pulse width, which was caused by the weakened self-heating effect. When the pulse width was set to be 500 μs, the NDR effect was almost negligible. Since the magnitude of NDR effect shows strong dependence on the pulse width, it can be confirmed that the NDR effect was mainly caused by the self-heating effect. The saturation current degradation increased with the vertical field, which was attributed to the stronger self-heating with higher output current. In this case, heat dissipation is of great importance to achieve high performance MoS_2 transistor due to the low thermal conductivity of MoS_2.

In summary, we fabricated high mobility MoS_2 field effect transistors with low Schottky barrier height contact by using 1–2 layers h-BN as a tunneling layer. Benefiting from the atomic thickness of h-BN, the Schottky barrier can be greatly reduced with small tunneling resistance. Increasing the h-BN thickness does not significantly influence the Schottky barrier height; however, it will increase the tunneling resistance. With the optimized h-BN thickness, the transistor with h-BN/Ni/Au contact shows a small Schottky barrier height of 31 meV and a low contact resistance of 1.8 kΩ·μm. Owing to the optimized tunneling contact, a typical FET showed a high field effect mobility of 73.0 cm^2 V^{-1} s^{-1} and output current of 330 μA μm^{-1} at room temperature, which can be further improved to 321.4 cm^2 V^{-1} s^{-1} and 572 μA μm^{-1} at 77 K, respectively. Overall, this MIS structure does not rely on low work function metals and phase engineered MoS_2, which makes it promising in practical application. The scalable CVD grown capability of h-BN enables large scale integration, which is crucial for future practical applications for high performance electronics.

Experimental Section

CVD Growth of h-BN on Cu Foils: The synthesis of h-BN was carried out in a horizontal tube furnace (22 mm inner diameter quartz tube) with a preposed heater using ammonia borane powder as the precursor. The temperature of the reaction zone was fixed at 1050 °C during CVD growth. Cu foils (0.025 mm, 99.8%, Alfa Aesar) were first polished, before growth of h-BN, the copper foil was annealed at 1050 °C for 20 min under 30 sccm hydrogen to grow the copper grain and to obtain a smooth surface. In a typical growth, the first heating zone is ramped up to 95 °C with a heating belt to produce the BN precursor. The second heating zone is heated up to 1050 °C for typically 10 min under 50 sccm hydrogen atmosphere, then the reaction was stopped by fast cooling.

CVD h-BN Transfer: The as-grown h-BN film on Cu foil was spin coated with Polymethylmethacrylate (PMMA) at 2000 rpm for 1 min and the back side was cleaned with O_2 plasma for 30 s. The Cu substrate was etched away by an aqueous solution of iron nitrate (0.05 g mL^{-1}) over a period of 12 h and then transferred into 10% HCl for 1 h. Finally, the film was washed with deionized water and placed on the target substrates and dried at 90 °C. In the end, PMMA was removed by acetone.

FET Fabrication and Characterization: The MoS_2 flake was mechanically exfoliated onto the SiO_2/Si (255 nm thick thermal oxide) substrate by the scotch tape method. CVD grown h-BN was transferred onto the substrate to cover the entire MoS_2 flake. Then the substrates were then spin coated with MMA and PMMA, and the EBL (JEOL 6510 with Nanometer Pattern Generation System) was employed to define the source and drain pattern. Metal contacts were then deposited using thermal deposition (15 nm Ni/50 nm Au contact and 50 nm Au contact) and electron beam deposition (15 nm Pd/50 nm Ag contact). Electrical performance of fabricated FETs was measured with the Lake Shore TTPX Probe Station and Agilent 4155C semiconductor parameter analyzer.

AFM Characterization: AFM imaging was performed by Bruker Multimode 8 with Scan Assist-Air probe under peak force mode in the ambient condition.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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