Low-Cost Energy-Efficient 3-D Nano-Spikes-Based Electric Cell Lysis Chips

Kashif Riaz, Siu-Fung Leung, Zhiyong Fan, *Member, IEEE*, and Yi-Kuen Lee, *Member, IEEE*

***Abstract*— Electric cell lysis (ECL) is a promising technique to be integrated with portable lab-on-a-chip without lysing agent due to its simplicity and fast processing. ECL is usually limited by the requirements of high power/voltage and costly fabrication. In this paper, we present low-cost 3-D nano-spikes-based ECL (NSP-ECL) chips for efficient cell lysis at low power consumption. Highly ordered HAR NSP arrays with controllable dimensions were fabricated on commercial aluminum foils through scalable and electrochemical anodization and etching. The optimized multiple pulse protocols with minimized undesirable electrochemical reactions (gas and bubble generation), common on micro parallel-plate ECL chips. Due to the scalability of fabrication process, 3-D NSPs were fabricated on small chips as well as on 4-in wafers. Phase diagram was constructed by defining critical electric field to induce cell lysis and for cell lysis saturation E_{sat} to define non-ECL and ECL regions for different pulse parameters. NSP-ECL chips have achieved excellent cell lysis efficiencies η_{lysis} (ca 100%) at low applied voltages (2 V), 2∼3 orders of magnitude lower than that of conventional systems. The energy consumption of NSP-ECL chips was 0.5-2 mJ/mL, 3∼9 orders of magnitude lower as compared with the other methods (5J/mL-540kJ/mL). [2016-0305]**

***Index Terms*— Nano-spikes, electric cell lysis chips, electrochemical anodization and etching processes, electric field enhancement, energy-efficient, lab on chip.**

I. Introduction

CELL LYSIS is an important step in sample preparation procedures and biopharmaceutical product extraction to release intracellular contents, i.e., DNA, RNA, hormones, vaccines, antibodies, recombinant proteins, and so forth. by disrupting cell membrane [1]–[6]. Economics of these procedures is greatly influenced by downstream processing steps, i.e., separation, purification, and so on. [1]. Sample preparation for molecular, protein and genomic diagnostic and analysis is time-consuming, labor intensive and costly process due to multiple steps and bulky instruments [4], [6]–[8]. Lab-on-a-chip (LOC) and micro total analysis system (μ -TAS) are rapidly growing in different fields ranging from molecular/protein/genome diagnostic and analysis to the search for life on Mars [9]–[13]. Due to recent developments in micro/nanotechnologies, conventional bulky and costly sample preparation processes can be scaled down and integrated into a single compact, automated, and portable microsystem, LOC or μ -TAS [4]–[12]. These microsystems have great promise due to their simplicity, low cost, time efficiency, low consumption of valuable reagents and biological samples [4]–[12].

Numerous techniques have been employed for cell lysis on integrated microsystems, LOC, or μ -TAS such as mechanical, chemical, thermal, ultrasonic, optical, electrical, with their unique advantages and limitations [2]–[7]. Mechanical cell lysis (MCL) based on exerting localized high pressure, shear stress, friction forces, compressive stress, on cell membrane through micro-channels, filters, moving membranes, beads, etc [2]–[5]. MCL integration on LOC is limited due to moving parts and blockage of micro/nanochannels, gaps, filters by cell debris [3]–[5]. Furthermore, due to cell debris micronization into small fragments and non-selective release of products through MCL; additional costly and time-consuming separation and purification steps are required [3]–[5]. Chemical cell lysis (CCL) utilized lysis agents such as surfactants, enzymes, detergents, etc., to dissolve cell membrane in microfluidic channel network [2]–[5]. CCL methods are limited due to pretreatment of lysing agents, purification of the added agents for downstream processing, different protocols for different samples and inherently slow due to complex chemical processes [3]–[5]. Thermal cell lysis utilized high temperatures and cyclic heating for cell lysis but not suitable for portable LOC systems due to high power requirement for heat generation and irreversible protein denaturation [3]–[5]. Ultrasonic cell lysis is not suitable for LOC systems due to complex instrumentation, excessive heat generation, and inefficient power transmission to samples [2]–[5]. Intracellular product yield greatly improved by increasing the intensity of cell lysis methods mentioned above, but it also increases micronization of cell debris and additional contaminants from intracellular compartments [1]. This increases the production cost and processing time due to additional downstream processing, i.e., separation, purification, etc. [1].

Electric Cell lysis (ECL) is a physical method that has potential to overcome these limitations due to its simplicity, cost effectiveness, high efficiency, fast processing, easy miniaturization, applicability to diverse samples, and possible

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TABLE I
COMPARISON OF MICRO/NANO ELECTRIC CELL LYSIS CHIPS

Ref.	Electrode	Amplitude (V)	Duration	Efficiency (%)	Remarks
[39]	3D Au/Ti micro	~8.5	-	74	Low efficiency
[40]	Pt/Ti micro	10-40	-	<80	Bubble generation
[18]	3D Au/Cr micro	10	-	30	Low efficiency
[38]	MWCNT	40	-	~100	High voltage
[14]	Cr/Au micro	20	100 µs	90	High voltage
[41]	Cr/Au micro	10	-	80	Low efficiency
[42]	Cr/Au micro	10	-	80	Low efficiency
[43]	ITO micro	30	-	61	Low efficiency
[44]	Cr/Au micro	5-6	5-10 min.	>95	Longer time
[45]	3D carbon micro	130	400 ms	90	High voltage
[46]	Pt/Ta micro	20	0.5-2 s	~100	High voltage
Our work	**3D Nano spikes**	**2**	**12ms**	**100±0.1**	**Low voltage High efficiency**

TABLE II
COMPARISON OF ELECTRIC CELL LYSIS ON ELECTRODES WITH AND WITHOUT NANOSTRUCTURES

Ref.	Nano-structures	Voltage requirement (V)	Without nano-structures (V)	Efficiency (%)
[38]	MWCNTs	40	85	100
[35]	CNTS	35	135	>95
[36]	CNTs	35	135	>95
[37]	CNTs	40	>90	100
[34]	Nano-gaped ITO electrodes	9	-	~90
this paper	3D Nano-spikes	2	>10	100±0.1

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integration with downstream processes as no lysis agents required [2]–[6], [14]. ECL employs intense pulsed electric field to induce irreversible nanopores on cell membrane which leads to cell lysis [2], [3]. ECL has been proved effective in avoiding complete cell disruption, micronization of cell debris and contaminants from intracellular compartments by selectively lysing the cell membrane rapidly and quickly [15]. Besides these advantages, ECL methods are limited by high energy consumption (5-500 J/mL) and voltage requirement (few tens of volts) as listed in Table 1 to achieve critical electric field for cell lysis E_{CL} (kV/cm). To fulfill these requirements, special costly and bulky power generators are necessary. This is highly undesirable in portable LOC applications [3], [4], [16]. Various designs have been proposed to achieve E_{CL} at low voltages either by decreasing the distance between electrodes or focusing electric field through small constriction segments and structures in microchannels or micro-chambers [2]–[4], [17]. Most commonly used 2D planar electrodes suffer from uneven exposure of cells to an electric field, resulting in low cell lysis efficiencies η_{lysis} [3], [16]. 3D electrodes were designed to overcome this drawback which showed higher η_{lysis} (30%) as compared to 2D electrodes (8%) [18]. However, the fabrication of 3D electrodes usually involves complex, time-consuming and costly fabrication steps [19], [20].

Direct current (DC) voltage is preferred as cell membrane experienced larger transmembrane potential (TMP) without lysing the intracellular components [3], [4], [17]. However, the voltage required to achieve electric field in kV/cm range usually lead to water electrolysis which may lead to gas bubble generation, extreme pH conditions and Joule heating [3], [21]. Alternating current (AC) voltages have been used to minimize these problems for on-chip ECL at optimized frequencies [3], [4], [21]. Depending on applied electric pulse amplitude, duration and number (usually high for ECL), AC ECL techniques also suffer from gas bubble generation, Joule heating, and pH variations [21]–[24]. These undesirable phenomena resulted in the production of unwanted electrolytic chemical compounds led to electrode degradation, effects on thermo-sensitive intracellular contents, i.e., proteins and on reaction kinetics of specific application [25]–[27]. To avoid these drawbacks, subcellular sized constriction structures were employed in a microchannel, so that maximum potential drop was across the cell membrane trapped in these structures instead of in the vicinity of the electrodes [28], [29]. The integration of these structures on portable LOC is limited by complex and costly manufacturing steps, expensive equipment for micro/nanoflow, channel blocking by cell debris and bubbles [3], [17], [25]–[27]. The average electric current between the electrodes can also be reduced by applying AC pulses with low amplitude and shorter duration. However, pulse parameters should be optimized to achieve high η_{lysis} in addition to the minimization of undesirable electrochemical reactions [21], [25], [30], [31]. Cell lysis efficiencies were always a concern in previous reports and η_{lysis} were well below 100% in most of the methods mentioned above [2], [3], [4] (Table 1).

High-aspect-ratio nano-structures (nano-tubes, nano-wires etc.) were incorporated on electrodes to locally enhance electric field intensity to cell membranes and used for cell lysis [32]–[37]. The cell lysing results on these chips indicated that required voltage reduced as compared to electrodes without nano-structures but still in the range of few tens of volts [32]–[37] (Table 2). One of the bottlenecks in the integration of nanostructures on microchips are the difficulties in handling, aligning and positioning the nanostructures at the exact desired location [46]. Furthermore, the fabrication techniques employed are complex, costly, time-consuming and non-reproducible [46]. It is highly desirable to establish simple, inexpensive, reliable and scalable fabrication techniques for fabrication of reproducible and aligned nanostructures to be used in integrated portable LOC systems and potential mass production [9], [46]–[48].

In this work, we present a low-cost 3D nano-spike based electric cell lysis chip which employed self-aligned highly

ordered 3D Aluminum (Al) nano-spike (NSP) arrays fabricated through electrochemical anodization and etching (EA&E) processes using anodic alumina membrane(AAM) as a template. 3D self-aligned highly ordered nano-structures were fabricated using EA&E processes recently due to their simplicity, low cost, reproducibility, and scalability [49]. These nano-structures showed enhanced performance in the field of electronics, optoelectronic, photovoltaic, magnetism, medical, and biology [49], [51]–[54]. Alumina is already recognized as bio-compatible material and used in hip arthroplasty [55], tissue engineering especially for skin replacement [56], bone implant [57], and cell culture and proliferation [58].

We developed an energy-efficient 3D nano-spikes based electric cell lysis (NSP-ECL) chips for efficient cell lysis at low energy consumption. NSP-ECL chips comprised of highly-ordered high-aspect-ratio (λ) 3D Al NSP arrays with controllable dimensions, i.e., length, L_{ns}, base radius, R_{ns}, and pitch, P_{ns} (spike to spike distance). These optimized aspect-ratio λ ($= L_{ns}/R_{ns}$) NSPs were fabricated on low-cost commercial Al foils through simple, scalable, reproducible and cost effective EA&E process. The electric field has been localized at NSPs due to high λ with an enhancement factor α. NSP-ECL chips have achieved high cell lysis efficiencies η_{lysis} (100%) at more than ten times reduced pulse amplitudes (2 V) through localized electric field E_{NSP} as compared to micron-distant parallel plate electric cell lysis (μ PPECL) chips without NSPs. The employment of low-cost EA&E fabrication process, optimized AC electric pulses with low amplitudes (2 V), short durations (few milliseconds) and low energy consumption (0.5-2 mJ/mL) minimized undesirable electrochemical reactions, such as gas and bubble generation on NSP-ECL chips. Due to the scalability of the fabrication process, 3D NSPs were fabricated on small chips as well as on wafers.

II. Nano-spikes Based Electric Cell Lysis System

Schematic diagram of a nano-spikes based electric cell lysis (NSP-ECL) system along with optical micrograph of fabricated nano-spikes on an Al foil and packaged NSP-ECL chip is shown Fig. 1. NSP-ECL chips consist of 3D periodic NSP arrays fabricated on a low-cost commercial Al foil using nano-imprint lithography, electrochemical processes, i.e., anodization and etching and MEMS technology. By controlling dimensions of NSPs, NSPs were fabricated with different aspect ratios λ ($= L_{ns}/R_{ns}$). Large λ resulted in electric field enhancement E_{ns} at NSPs and applied electric field E_a was enhanced with an enhancement factor α. A PCI 6110 DAQ card (National Instrument, TX, USA) and a Labview program were used to apply AC electric pulses with adjustable pulse amplitudes V_a, durations t_p and number P_n to NSP-ECL chips. An Olympus IX70 inverted fluorescent microscope, and a QImaging Retiga 1300C digital CCD camera (Burnaby, B.C., Canada) were used to acquire a set of bright field and fluorescent micrographs before and after ECL through an image capture card. Cell lysis efficiency η_{lysis} were determined as functions of electric pulse parameters (V_a, t_p and P_n) and NSPs dimensions using these acquired images through image processing. Due to E_{ns} and optimized

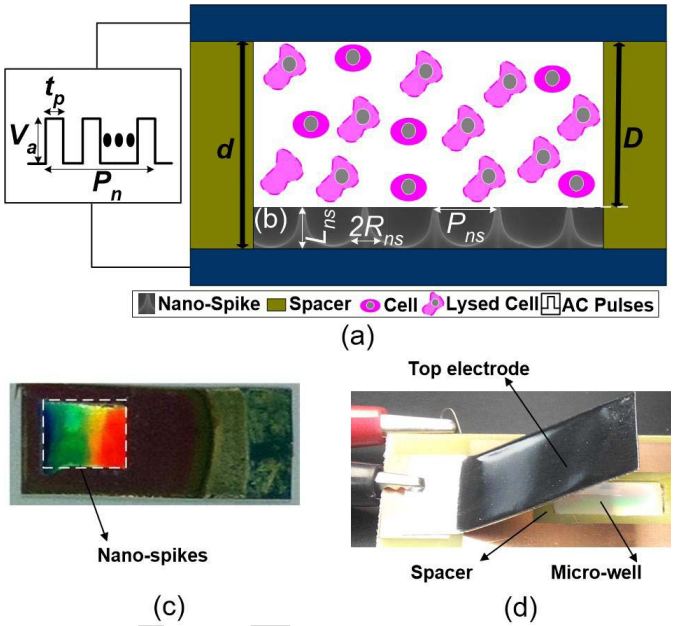

Fig. 1. Illustration of a Nano-Spikes Electric Cell Lysis (NSP-ECL) device, (a) the schematic diagram of an NSP-ECL chip with NSP arrays, (b) SEM micrograph of an array of nano-spikes, (c) optical micrograph of an Al foil with fabricated nano-spikes, and (d) optical micrograph of packaged NSP-ECL chip.

electric pulse parameters, NSP-ECL chips offer the advantage of achieving high η_{lysis} at reduced pulse amplitudes and shorter pulse durations. ECL with low pulse amplitudes and shorter pulse durations minimized undesirable electrochemical reactions such as gas and bubble generation and avoided complete disruption and micronization of cell membrane which is desirable in downstream process integration on LOC system.

A. Nano-Spikes Based Electric Cell Lysis Chip Design

3D periodic NSP arrays on a microchip were fabricated through electrochemical anodization and etching processes. 3D NSPs were fabricated with different controllable dimensions, such as length, L_{ns}, base radius, R_{ns}, and pitch, P_{ns}(spike to spike distance). The top and bottom electrodes are insulated by a spacer (3M Orange Polyimide electrical insulation tape) with a thickness d ($= 100\mu$m). The distance between the tip of the NSPs and the counter electrode of the NSP-ECL chip is defined as D ($= d - L_{ns}$). This spacer not only insulated two electrodes, but also formed a micro-well between two electrodes for cell sample and molecules injection (Fig. 1(a)). The incorporation of optimized aspect-ratio λ NSPs resulted in enhancement of applied electric field. The electric field at NSPs E_{ns} was enhanced by enhancement factor α which depends on the aspect ratio of NSPs. The top electrode of NSP-ECL chip is removable, and cell lysate can be collected from micro-well after electric cell lysis using a pipette.

B. 3D Nano-Spikes Fabrication Process

Major steps involved in the fabrication of NSP-ECL chips were nano-imprinting and scalable electrochemical anodization and etching processes [31], [51]–[54], [59]. First of all, low-cost commercially available *ca* 250 μm thick

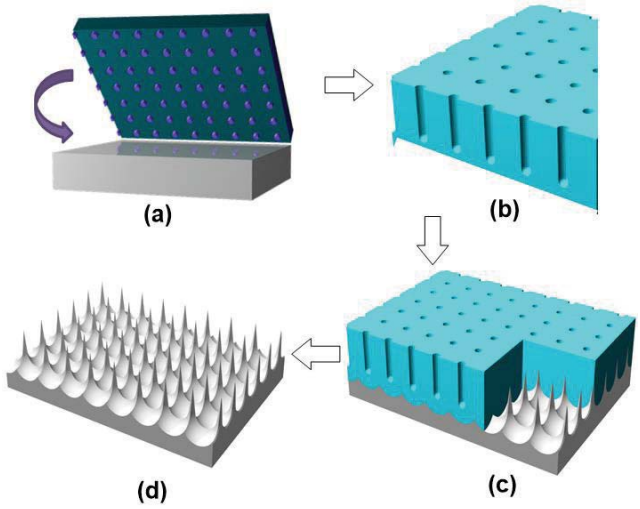

Fig. 2. Key fabrication processes of low-cost highly-ordered 3D nano-spike arrays using electrochemical anodization and etching processes, (a) Al foil was imprinted by a silicon mold with squarely patterned pillars, (b) imprinted Al foil with periodic nanoholes, (c) imprinted substrate was anodized and then etched to fabricate 3D nano-spike arrays, and (d) 3D high aspect-ratio nano-spike arrays fabricated through electrochemical anodization and etching processes.

Al foils (99.99% Alfa Aesar, MA, USA) were cut into pieces of 2×1 cm^2. These Al substrates were cleaned with acetone and then rinsed with isopropyl alcohol and deionized (DI) water. These cleaned substrates were electrochemically polished for 4 minutes at 5°C in a 1:3 (v:v) mixture of perchloric acid and ethanol. A silicon stamp with squarely patterned pillars with a height of ∼200 nm, the diameter of ∼200-500 nm and pitch of 1.2 μm was used for nano-imprinting (Fig. 2(a)). The electropolished substrates were imprinted by the stamp and substrates had perfect squarely ordered nano-indentation which defined the location of the anodic alumina membrane (AAM) pores (Fig. 2(b)). The imprinted substrates were then anodized in a home-built anodization setup using carbon rod as counter electrode using DC voltage of 600 V. The composition of electrolyte used for anodization was 1:1 (v:v) 2wt% Citric acid: Ethylene Glycol + 9 mL 0.1wt% Phosphoric acid. NSPs with different aspect ratios were fabricated by controlling anodization conditions, i.e.; anodization time varies between 30-360 minutes at 10°C. Stability of electrolyte was improved by mixing citric acid with ethylene glycol, and the anodization voltage was increased up to 600 V [51]–[54]. The mixture of phosphoric acid (6%) and chromic acid (1.5%) was used to etch the anodized AAM layer at 100°C for 25 minutes to obtain perfectly ordered 3D NSP arrays (Fig. 2(c)). After etching, the 3D Al NSP electrodes were rinsed with DI water and blown dry with compressed air.

C. Scalability of Nano-Spikes Fabrication Process

The dimensions of NSPs were precisely controlled by controlling the parameters and conditions of EA&E process, i.e., the thickness of AAM, anodization time, etc. NSPs with different lengths L_{ns} ranging from 350-1100 nm was fabricated by increasing anodization time from 30-360 minutes. The maximum achievable L_{ns} was about ∼1100 nm after anodization of 360 minutes. SEM images of NSP array electrodes with L_{ns} of 350, 750, and 1100 nm with pitch P_{ns} of 1.2 μm are shown in Fig. 3. Several advantages are associated with NSPs fabricated using EA&E processes such as periodicity, self-organization, scalability, reproducibility, and high-aspect-ratio λ. Due to the scalability of above mentioned EA&E fabrication process, it was possible to fabricate NSPs on low-cost Al foils for microchips as well as on 4-inch glass wafers (Fig. 4). The sample in microliter range was processed on 3D NSP-ECL chips, while throughput can be scaled up to handle large cell populations ($10^4 - 10^5$) on NSP-ECL wafers. This simple, low-cost, scalable, reproducible and reliable process is highly attractive for low energy and cost-effective portable μ -TAS, LOC and smartphone-based systems as well as for high throughput and large population applications.

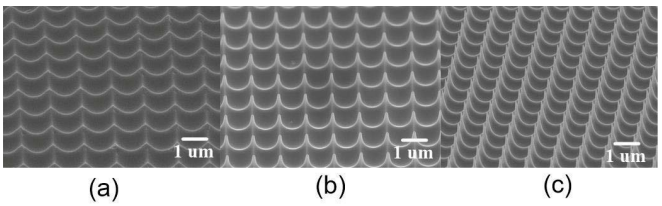

Fig. 3. SEM micrograph of 3D nano-spike arrays with different lengths L_{ns} of (a) 350 nm, (b) 750 nm, and (c) 1100 nm.

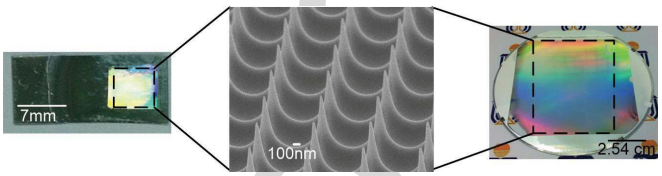

Fig. 4. Highly-ordered 3D nano-spike arrays fabricated on low-cost commercial Aluminum foil with an area of 7mm^2 and also on a 4-inch glass wafer.

III. Material and Methods

A. Cell Line Preparations

Human cervical cancer (HeLa) cell line was used in the ECL experiments to characterize cell lysis efficiencies η_{lysis} on NSP-ECL chips. HeLa cells were cultured and grown in Eagle's minimal essential medium (EMEM) (CCL-2™, ATCC, VA, USA), supplemented with 10% fetal bovine serum (FBS) (ATCC, VA, USA) and 1% Streptomycin/Penicillin (GIBCO®, Invitrogen Inc., USA) at 37°C and 5% CO_2. To perform the ECL experiments on the NSP-ECL chips, HeLa cells were re-suspended in the Phosphate buffered saline (PBS). Then, the EMEM medium was sucked, washed twice with PBS and trypsinized by 0.25% trypsin/EDTA (GIBCO®, Invitrogen Inc., USA) for 3-5 minutes at 37 °C. The detached cells were centrifuged at 1,200 rpm at room temperature for 3 minutes. The concentration of HeLa cells was adjusted to 1×10^5 cells/mL in suspension.

B. Dual Acridine Orange/Ethidium Bromide Fluorescent Staining

Cell lysis efficiencies η_{lysis} is defined as the percentage of dead cells after application of a lysing electric field [44].

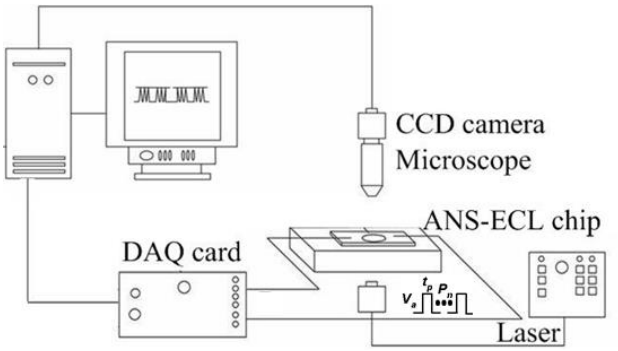

Fig. 5. The schematics of the experimental setup to perform the electric cell lysing on the fabricated NSP-ECL chips.

η_{lysis} can be determined by using dual fluorescent dye staining using Acridine Orange and Ethidium Bromide (AO/EB; Sigma, St Louis, MO, USA) which are nuclear staining dyes [60]–[62]. Acridine Orange (AO) is a membrane permeable dye and emits green fluorescence while Ethidium Bromide (EB) is membrane-impermeable dye and emits red fluorescence after entering the cell through compromised membranes. Upon staining cells with dual AO/EB dyes, live cells emit green fluorescence while lysed cells with damaged membrane emit orange-yellow fluorescence [60]–[62]. To determine η_{lysis}, the cell suspension was injected to the NSP-ECL chips and the electric pulses were applied. False readings from the reversibly electroporated cells were avoided by adding dual AO/EB staining solution to the cell suspension 5 minutes after the application of electric pulses on the NSP-ECL chips. Lysed cells exhibited orange-yellow fluorescence when EB dye bind with DNA/RNA either inside or outside the cell through the ruptured cell membrane. η_{lysis} was calculated by counting cells that appeared orange-yellow under fluorescence over the entire cells.

C. Experimental Setup

A PCI 6110 DAQ card (National Instrument, TX, USA) and a Labview program were used to apply electric pulses with adjustable pulse amplitude (V_a), pulse duration (t_p) and pulse number (P_n) to the NSP-ECL chip as shown in Fig. 5. The cell's response before and after ECL was observed using an Olympus IX70 inverted fluorescent microscope and a QImaging Retiga 1300C digital CCD camera (Burnaby, B.C., Canada) (Fig. 5). Sets of bright field and fluorescence micrographs were acquired by an image capture card. These digital images were processed to determine the η_{lysis} as a function of electric pulse parameters on NSP-ECL chips.

D. Statistical Analysis

At least 100 cells were analyzed to obtain each data point, and each experiment was repeated at least three times. The standard deviation between repeated experiments was shown as error bars.

IV. Electric Field Enhancement

Electric field distribution was simulated to evaluate the electric field enhancement at NSPs. A commercial finite element method (FEM) package (COMSOL Multiphysics 4.2, COMSOL Ltd., USA) was used for electric field distribution simulations [63]. The profile of NSPs was extracted with the help of extract profiles tool using the AFM images of NSPs. The extracted coordinates of NSPs were then exported to COMSOL. The cell lysis chamber is *ca* 100 μm high (the distance between the top and bottom electrode). The top electrode and the tip of the spikes on the bottom electrode were separated by a distance D (99 μm) and the space between the two electrodes was considered as cell suspension medium (Fig. 6). The relative permittivity and conductivity of cell suspension medium were assumed to be 77.4 $\pm$ 5% and 1.7 S/m $\pm$ 10%, respectively [59]. The fixed potential between the electrodes was used as the boundary condition. The fixed potential between the electrodes was applied by selecting 2D stationary electrostatics physics in COMSOL. These simulations demonstrated that applied electric field E_a is enhanced and defined by enhancement factor α which on the other hand highly depend on the aspect ratio λ of NSPs. The enhanced electric field E_{ns} is very large near tips of NSPs and E_{ns} become uniform few nm above 3D NSP arrays as shown in Fig. 6.

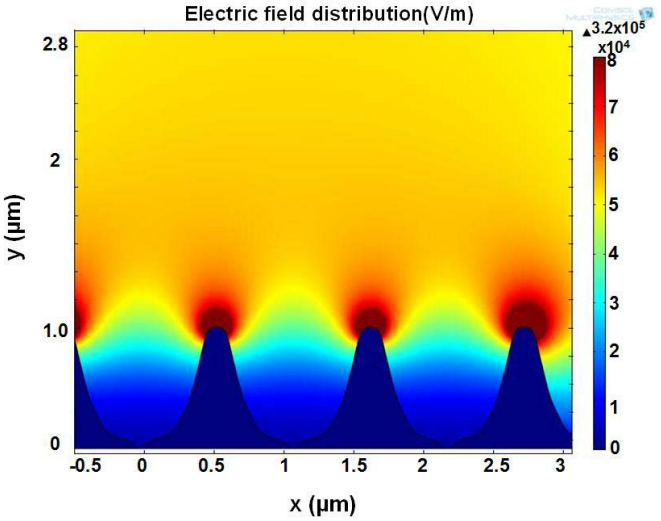

Fig. 6. Numerical simulation of the electric field distribution between nano-spike array electrodes using COMSOL at $V_a = 4$V. The simulation shows local electric field enhancement, especially near the nano-spikes.

The enhanced electric field E_{ns} was localized on NSPs due to the optimized aspect ratioλ of NSPs. The enhancement factor α by which the applied electric field E_a is enhanced can be estimated using the following relation [64], [65]:

$$E_{ns} = E_a \times \alpha \times \gamma \quad (1)$$

where E_a is the applied electric field (V_a/D), α is the enhancement factor and γ is the correction factor to incorporate the electrochemical impedance near the fluid-electrode interface and determined through electrochemical impedance spectroscopy [66], [67]. Based on the geometries of nanostructures, several models have been proposed to estimate α [65]. In our case, the α was estimated by considering NSP as a hemi-ellipsoid with length L_{ns} and base radius R_{ns} as

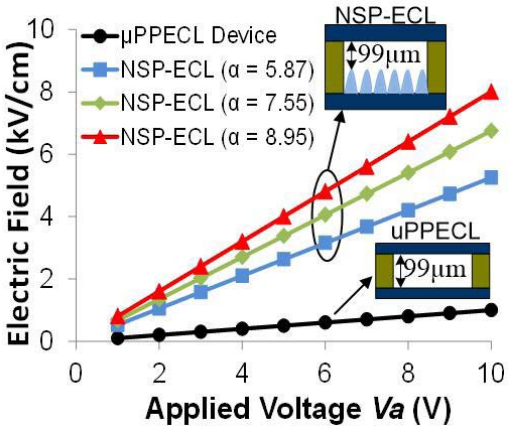

Fig. 7. Electric field as a function of applied voltages V_a for micro parallel plate electric cell lysing (μ PPECL) device without nano-spikes and NSP-ECL devices with different α.

follows [65]:

$$\alpha = \xi^3/[\{\lambda ln(\lambda + \xi)\} - \xi] \quad (2)$$

where $\xi = (\lambda^2 - 1)^{1/2}$ and λ is the aspect ratio of NSP (L_{ns}/R_{ns}). It is evident from (2) that α is a function of λ and α can increase exponentially with increasing λ. λ. As mentioned previously, the aspect ratio λ can be controlled by controlling dimensions of NSPs. We have successfully fabricated NSPs with λ up to 3 using EA&E process. For NSPs with L_{ns} of 1100nm, the R_{ns} was 375nm which leads to the aspect ratio of around 3. For NSPs with λ ranging between 2 and 3, α was estimated between 5.9 and 8.9 using Equation (2). For micron-distant parallel plate electric cell lysis (μ PPECL) devices without NSPs, the electric field E_{planar} can be estimated as the ratio of applied voltage V_a to the distance between parallel plate electrodes $D(E_{planar} = V_a/D)$. Interelectrode distance D of ~99 μm was considered for both μ PPECL and NSP-ECL devices to compare electric field. Enhanced electric field at NSPs E_{ns} was determined using (1) and (2). The electric field was enhanced at NSP-ECL devices by enhancement factor α as compare to μ PPECL devices (Fig. 7). This means that lower voltages are required to achieve a specific electric field on the NSP-ECL devices depending on α as compared to μ PPECL devices. For example, electric field of 2 kV/cm can be achieved at 20 V for μ PPECL device, at ~4 V for NSP- ECL device with α of 5.87, at ~3 V for NSP- ECL device with α of 7.55 and at ~2.6 V for the NSP-EP ECL device with α of 8.95 (Fig. 7).

V. Results and Discussion

When a cell is exposed to an externally applied electric field, localized transient microstructural changes and nanopore generation takes place in the cell membrane. These changes and induced nano-pores can either resealed (reversible electroporation) or non-resealed (irreversible electroporation) depending on applied electric pulse parameters V_a, t_P and P_n [34]–[37]. Irreversible electroporation causes rupturing of the cell membrane and cell lysis due to dielectric breakdown of the cell membrane as cell unable to maintain essential ionic balance across the membrane. ECL occurs only when applied electric pulse parameters V_a, t_P and P_n are well above their critical values [4]. Irreversible nano-pore generation is initiated when an electric field is well above its critical value E_{CL} which in turn determined by pulse amplitude V_a and density and duration of these nanopores depend on t_P and P_n [34]–[37]. It is critical to optimize these electric pulse parameters to achieve high η_{lysis} at low energy consumption to avoid undesirable electrochemical reactions and possible integration with portable devices. In our ECL experiments, we have applied rectangular AC pulses with adjustable V_a of 1–10 V, t_P of 1–12 ms and P_n of 1-10 on NSP-ECL chips with α of 5.87, 7.55 and 8.95.

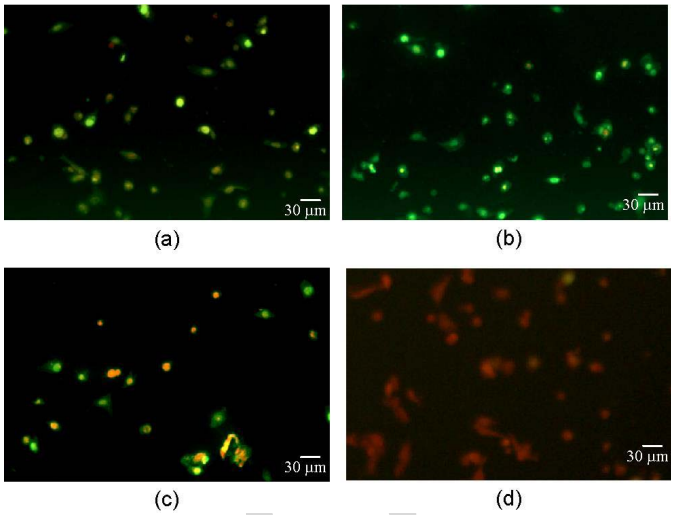

Fig. 8. Fluorescence micrographs of Acridine orange and Ethidium bromide dual stained HeLa cells treated on NSP-ECL chips and μ PPECL devices. Viable cells exhibit green fluorescence while lysed cells exhibit orange-red fluorescence due to loss of membrane integrity. (a) HeLa cells undergone electric cell lysis (ECL) on μ PPECL without nano-spikes at pulse amplitude $V_a = 5$V and pulse duration $t_P = 12$ms, (b) HeLa cells before ECL on NSP-ECL chips ($\alpha = 8.9$), (c) HeLa cells after ECL on NSP-ECL chips ($\alpha = 8.9$) at $V_a = 2$V and $t_P = 10$ms, and (d) HeLa cells after ECL on NSP-ECL chips ($\alpha = 8.9$) at $V_a = 2$V and $t_P = 12$ms.

A. Fluorescence Microscopy

Cell lysis efficiencies were quantified by using dual AO/EB fluorescent staining (Fig. 8). Fluorescence micrographs of cells before ECL on NSP-ECL chips showed no yellow-orange fluorescence as cell membrane was intact and impermeable to EB dye molecules (Fig. 8(b)). After ECL, cell membrane ruptured due to induction of irreversible nanopores on cell membranes by applied electric field. EB molecules entered the cells through compromised membrane and stained the lysed cells. Lysed cells exhibited orange-red fluorescence, while the live cells emitted green fluorescence (Fig. 8(c) & (d)). Almost all cells exhibited orange-red fluorescence when lysed on NSP-ECL chips at 2 V and 12 ms pulses showing high η_{lysis}. Fluorescence micrograph of ECL on μ PPECL devices at 5 V and 12 ms pulses showed almost no orange-red fluorescence showing very low η_{lysis} (Fig. 8(a)).

B. Enhancement Factor Effect on Electric Cell Lysis

Cell lysis efficiencies were quantified on NSP-ECL chips with different α and on μ PPECL devices in order to determine

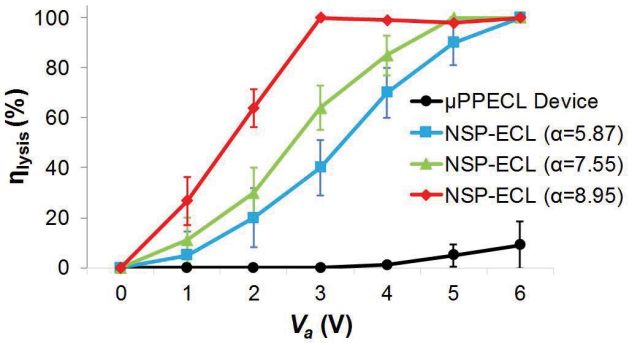

Fig. 9. Cell lysis efficiency η_{lysis} as a function of applied pulse amplitude V_a on NSP-ECL chips with different α (5.9, 7.5, 8.9) and the cell lysis efficiency of the μ PPECL device for pulse duration t_P of 10ms.

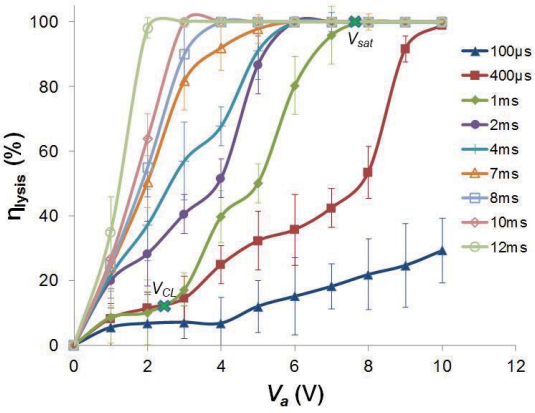

Fig. 10. Cell lysis efficiency η_{lysis} as a function of V_a and t_P for P_n of 10 on NSP-ECL chip.

the effect of α on η_{lysis} as compared to μ PPECL devices without NSPs. From Fig. 9, it is clear that cell lysis on NSP-ECL chips showed higher η_{lysis} as compared to cell lysis on μ PPECL devices at specific V_a due to enhanced electric field E_{ns} on NSPs. At $V_a = 3$ V, the η_{lysis} was 40 to 100% high on NSP-ECL chips as compared to μ PPECL devices depending on enhancement factor $\alpha$of NSP-ECL chips. η_{lysis} was increased with increasing α on NSP-ECL chips at specific V_a. η_{lysis} of 40%, 64% and 100% were achieved at $V_a = 3$ V on NSP-ECL chips with α of 5.87, 7.55 and 8.95 respectively. NSP-ECL chips with α of 8.95 was selected for further analysis due to high η_{lysis} at low voltages.

C. Critical Values for Electric Cell Lysis

Based on the applied electric field, ECL process can be divided into three phases as shown in Fig. 10. When the applied electric field is below critical electric field E_{CL}, η_{lysis} is very low as the electric field is not sufficient to induce enough irreversible nano-pores rather reversible nanopores on the cell membrane. When the applied electric field was above E_{CL}, the electric field was strong enough to break down the integrity of cell membrane by inducing enough irreversible nano-pores. EB fluorescent molecules bound to DNA/RNA inside or outside the ruptured cell membrane and lysed cells exhibited orange-red fluorescence (Fig. 8(c) and (d)). At this stage, a small increase in pulse amplitude V_a, more and more cells lysed and η_{lysis} increased quickly (Fig. 10). η_{lysis}keep on increasing by increasing electric field until η_{lysis} saturated and electric field at this point defined as saturation electric field E_{sat}(Fig. 10). Further increase in V_a did not improve η_{lysis} but increased power consumption.

D. Electric Pulse Parameters Effects on Electric Cell Lysis

The cell lysis efficiencies were greatly influenced by applied electric pulse parameters such as V_a, t_P and P_n. Higher η_{lysis} can be achieved at higher pulse amplitude V_a, longer pulse duration t_p and higher pulse number P_n(Fig. 10). Higher pulse amplitude V_a and longer pulse duration t_p increased power requirement and may also induce undesirable electrochemical reactions. Electric pulse parameters should be optimized to achieve high η_{lysis} but at lower V_a and shorter $t_p$to minimize electrochemical reactions and power requirement. We have reached high η_{lysis}(∼100%) at V_a of 2 V, t_p of 12 ms and P_n of 10 on NSP-ECL chip (Fig. 10). This reduction in V_a is more than ten times lower as compared to μ PPECL devices.

E. Energy Requirement for Electric Cell Lysis

The energy consumption for electric cell lysis is a crucial issue especially in LOC, μ -TAS and smartphone based microsystems where limited energy is available [3], [68]. This energy requirement is high enough to employ complex, bulky and costly power generators and equipment [16], [69]. Due to high energy requirement, ECL systems usually undergo metal ion dissolution, local pH variation, Joule heating, gas and bubble generation and sample contamination [3], [4], [5], [17], [25], [68], [70]. In order to avoid these undesirable reactions on ECL devices and to integrate them on LOC, μ-TAS and smartphone based microsystems; low energy consumption ECL systems are highly desirable. In our approach, we utilized 3D nano-spikes on which electric field was enhanced due to their optimized aspect-ratio. We were able to achieve cell lysis at lower pulse amplitudes due to electric field enhancement. The specific energy input W delivered to samples on NSP-ECL chips was calculated using relation:

$$W = V_a I P_n . t_p / vol \quad (3)$$

where V_a is the applied pulse amplitude, I is the electric current, P_n is the pulse number, t_p is the pulse duration, and vol is the sample volume (0.25 mL). A high-precision 1kΩ resistor was connected in series with the chip and serve as the current-to-voltage converter. The resistance of the resistor is too small as compared to the chip. Therefore, it can be ignored in the electric current calculation. The voltage signals from this resistor were measured by using a PCI 6110 DAQ card (National Instrument, TX, USA) and a Labview program and used in the electric current calculation. The specific energy input W required to achieve optimized electric pulse protocol (2V × 12ms for 10 pulses) was 0.5 mJ/mL (Fig. 11). The energy consumption for cell lysis on NSP-ECL

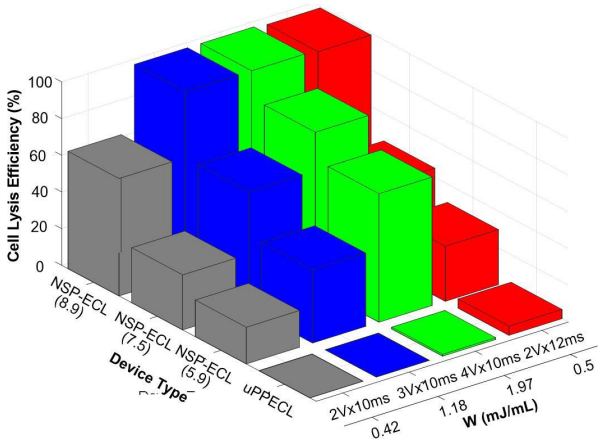

Fig. 11. η_{lysis} for different NSP-ECL and μ PPECL devices as a function of different electric pulse protocols and specific energy input W (mJ/mL).

TABLE III
SPECIFIC ENERGY REQUIREMENT FOR CELL LYSIS USING DIFFERENT METHODS

Ref.	Methods	Device characteristics	Treatment time	Specific energy input
[72]	Laser	Beam dia. of 100µm	60sec × 10 times	16kJ/mL
[72]	Microwave	1025W 2.45GHz	20min.	74.6kJ/mL
[72]	Mechanical solid shear	Blade dia. 40mm 120W, 3000 rpm	6min.	540kJ/mL
[72]	Thermal lysis	90^0C	20min.	20.1 kJ/mL
[72]	Liquid shear ultrasonication	40W ultrasonic bath	20min.	132 kJ/mL
[73]	High voltage pulsed electric field	$L\times W$=30×3mm^2 d = 10mm	1µs	100-200 J/mL
[74]	Electroporation	A=0.78cm^2 d = 0.3cm	µs-ms	16-150 J/mL
[75]		$L\times W$:2.8×0.6cm^2 d = 1mm	100µs × 32	5-533 J/mL
This paper	NSP-ECL device	NSP dimensions L: 350-1100nm D: 200-500nm	12ms × 10	0.05-3 mJ/mL

$L\times W$: electrode length × width, d: interelectrode distance, A: electrode area, D: diameter

chips was 0.5-2 mJ/mL that is 3-9 orders of magnitude lower as compared to other cell disintegration methods as shown in Table 3.

Low device reliability and failure were observed in macro and micro ECL devices due to high voltage operations which resulted in electrolysis, gas bubble generation, Joule heating, local pH variations, etc. [21]–[27]. Electrode degradation and cell damage were observed during electroporation and ECL processes due to gas bubbles generation which resulted in local pH variations and violent hydrodynamic forces [21]–[24], [59]. Gas bubble generation was observed on micro devices due to high voltage operation especially above 6 V [22], [75] as shown in Fig. 12(b). Although AC pulses were applied on micro devices which were known to minimize electrochemical reactions, still applied pulse amplitudes were high

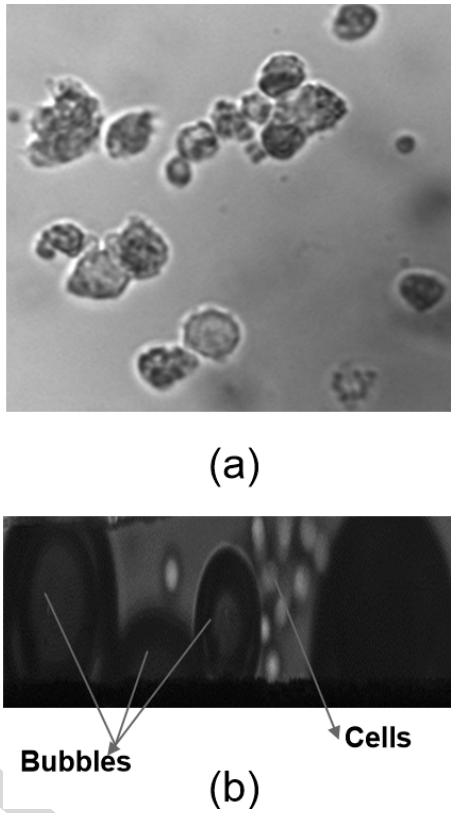

Fig. 12. Cell morphologies after electric cell lysis on (a) NSP-ECL chips, bubble generation, and cell micronization was avoided and (b) on a micro ECL chip, Bubble generation was observed on micro devices [22], [75].

enough to induce gas bubble generation and electrode degradation (Fig. 12 (b)). On the other hand, on NSP-ECL chips, due to the employment of NSPs, high η_{lysis} was achieved at low pulse amplitudes without bubble generation (Fig. 12(a)). In addition, the cell membrane was not fully disintegrated after ECL on NSP-ECL chips (Fig. 12(a)). This will avoid micronization of cell debris and complex, costly and time-consuming downstream processes.

F. Phase Diagram for Electric Cell Lysis

ECL occurs successfully when applied electric field is well above its critical value E_{CL}. It is crucial to determine electric pulse parameters to achieveE_{CL} as if the electric field is below this critical value; cells will be reversibly electroporated instead of lysed. E_{CL} was achieved at different V_a for different t_p, at lower V_a for longer t_p, and at higher V_a for shorter t_p. E_{CL} is defined as a critical electric field for cell lysis which induces irreversible nanopores on the cell membrane and η_{lysis} increases quickly. We have also determined electric pulse parameters to achieve saturation electric field E_{sat} at which η_{lysis} saturated. It is vital to determine E_{sat} as increasing pulse parameters after this point will only result in additional power hence energy consumption and micronization of cell debris which is not suitable for portable LOC systems and downstream processes. Using these parameters for E_{CL} and E_{sat}, we have constructed "phase diagram" for ECL of HeLa cells on NSP-ECL chips (Fig. 13). Phase diagram defines

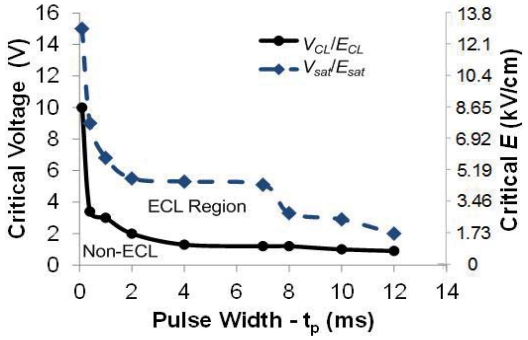

Fig. 13. The Phase diagram for the electric cell lysis of HeLa cells on the NSP-ECL chip ($\alpha = 8.9$). The Phase diagram shows the non-ECL and ECL regions for different applied pulse durations.

the boundary for non-ECL and ECL regions for different electric pulse parameters. Minimum pulse amplitude $V_{CL,min}$ to achieve E_{CL} was 0.9 V for t_p of 12 ms which is more than thirteen times lower as compared to μ PPECL devices. Minimum pulse amplitude $V_{sat,min}$ to achieve E_{sat} was 2 V for t_p of 12 ms which is more than ten times lower as compared to μ PPECL devices.

VI. Conclusion

In conclusion, we have developed a low-cost energy-efficient 3D nano-spike based electric cell lysis (NSP-ECL) chips for efficient cell lysis at low pulse amplitudes and duration. Highly-ordered self-aligned 3D Al NSP arrays with controllable dimensions, i.e., length, L_{ns}, base radius, R_{ns}, and pitch, P_{ns} (spike to spike distance) were fabricated on low-cost commercial Al foils through simple, scalable, reproducible and cost effective electrochemical anodization and etching processes. The electric field has been localized at NSPs due to optimized aspect-ratio with an enhancement factor α as compared to micro-distant parallel plate electric cell lysis (μ PPECL) chips without NSPs. NSP-ECL chips have achieved high cell lysis efficiencies η_{lysis} (100%) at more than ten times reduced pulse amplitudes (2 V) through localized electric field E_{ns} as compared to the μ PPECL chips without NSPs. These applied pulse amplitudes are 2-3 times reduced as compared to traditional electroporation systems used for different applications. The specific energy input required to achieve 100% η_{lysis} was only in the range of 0.5-2 mJ/mL which is 3-9 orders of magnitude lower as compared to other cell disintegration methods (5J/mL-540kJ/mL). The employment of NSPs fabricated through low-cost EA&E process, optimized AC electric pulses with low amplitudes and short durations minimized undesirable electrochemical reactions, such as gas and bubble generation on NSP-ECL chips which were observed on micro devices due to high voltage operation. Due to the scalability of the fabrication process, 3D NSPs were fabricated on small chips as well as on wafers to process samples for microsystems as well as for high throughput applications. These energy-efficient NSP-ECL chips are highly attractive for integration with other sample preparation downstream processes on portable LOC and μ-TAS systems due to its low power consumption, reliability, cost-effectiveness and avoiding micronization of cell debris. Based on these low voltage devices, we can add additional ECL tool in a recently developed "Lab on Smartphone" through which optimized EP protocols can be applied to micro/nano EP chips through an open-source MCU (Arduino) with an integrated Bluetooth module [48].

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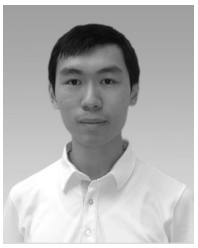

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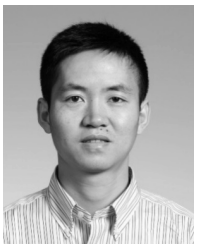

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Low-Cost Energy-Efficient 3-D Nano-Spikes-Based Electric Cell Lysis Chips

Kashif Riaz, Siu-Fung Leung, Zhiyong Fan, *Member, IEEE*, and Yi-Kuen Lee, *Member, IEEE*

***Abstract*— Electric cell lysis (ECL) is a promising technique to be integrated with portable lab-on-a-chip without lysing agent due to its simplicity and fast processing. ECL is usually limited by the requirements of high power/voltage and costly fabrication. In this paper, we present low-cost 3-D nano-spikes-based ECL (NSP-ECL) chips for efficient cell lysis at low power consumption. Highly ordered HAR NSP arrays with controllable dimensions were fabricated on commercial aluminum foils through scalable and electrochemical anodization and etching. The optimized multiple pulse protocols with minimized undesirable electrochemical reactions (gas and bubble generation), common on micro parallel-plate ECL chips. Due to the scalability of fabrication process, 3-D NSPs were fabricated on small chips as well as on 4-in wafers. Phase diagram was constructed by defining critical electric field to induce cell lysis and for cell lysis saturation E_{sat} to define non-ECL and ECL regions for different pulse parameters. NSP-ECL chips have achieved excellent cell lysis efficiencies η_{lysis} (ca 100%) at low applied voltages (2 V), 2∼3 orders of magnitude lower than that of conventional systems. The energy consumption of NSP-ECL chips was 0.5-2 mJ/mL, 3∼9 orders of magnitude lower as compared with the other methods (5J/mL-540kJ/mL). [2016-0305]**

***Index Terms*— Nano-spikes, electric cell lysis chips, electrochemical anodization and etching processes, electric field enhancement, energy-efficient, lab on chip.**

I. Introduction

CELL LYSIS is an important step in sample preparation procedures and biopharmaceutical product extraction to release intracellular contents, i.e., DNA, RNA, hormones, vaccines, antibodies, recombinant proteins, and so forth. by disrupting cell membrane [1]–[6]. Economics of these procedures is greatly influenced by downstream processing steps, i.e., separation, purification, and so on. [1]. Sample preparation for molecular, protein and genomic diagnostic and analysis is time-consuming, labor intensive and costly process due to multiple steps and bulky instruments [4], [6]–[8]. Lab-on-a-chip (LOC) and micro total analysis system (μ -TAS) are rapidly growing in different fields ranging from molecular/protein/genome diagnostic and analysis to the search for life on Mars [9]–[13]. Due to recent developments in micro/nanotechnologies, conventional bulky and costly sample preparation processes can be scaled down and integrated into a single compact, automated, and portable microsystem, LOC or μ -TAS [4]–[12]. These microsystems have great promise due to their simplicity, low cost, time efficiency, low consumption of valuable reagents and biological samples [4]–[12].

Numerous techniques have been employed for cell lysis on integrated microsystems, LOC, or μ -TAS such as mechanical, chemical, thermal, ultrasonic, optical, electrical, with their unique advantages and limitations [2]–[7]. Mechanical cell lysis (MCL) based on exerting localized high pressure, shear stress, friction forces, compressive stress, on cell membrane through micro-channels, filters, moving membranes, beads, etc [2]–[5]. MCL integration on LOC is limited due to moving parts and blockage of micro/nanochannels, gaps, filters by cell debris [3]–[5]. Furthermore, due to cell debris micronization into small fragments and non-selective release of products through MCL; additional costly and time-consuming separation and purification steps are required [3]–[5]. Chemical cell lysis (CCL) utilized lysis agents such as surfactants, enzymes, detergents, etc., to dissolve cell membrane in microfluidic channel network [2]–[5]. CCL methods are limited due to pretreatment of lysing agents, purification of the added agents for downstream processing, different protocols for different samples and inherently slow due to complex chemical processes [3]–[5]. Thermal cell lysis utilized high temperatures and cyclic heating for cell lysis but not suitable for portable LOC systems due to high power requirement for heat generation and irreversible protein denaturation [3]–[5]. Ultrasonic cell lysis is not suitable for LOC systems due to complex instrumentation, excessive heat generation, and inefficient power transmission to samples [2]–[5]. Intracellular product yield greatly improved by increasing the intensity of cell lysis methods mentioned above, but it also increases micronization of cell debris and additional contaminants from intracellular compartments [1]. This increases the production cost and processing time due to additional downstream processing, i.e., separation, purification, etc. [1].

Electric Cell lysis (ECL) is a physical method that has potential to overcome these limitations due to its simplicity, cost effectiveness, high efficiency, fast processing, easy miniaturization, applicability to diverse samples, and possible

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TABLE I
COMPARISON OF MICRO/NANO ELECTRIC CELL LYSIS CHIPS

Ref.	Electrode	Amplitude (V)	Duration	Efficiency (%)	Remarks
[39]	3D Au/Ti micro	~8.5	-	74	Low efficiency
[40]	Pt/Ti micro	10-40	-	<80	Bubble generation
[18]	3D Au/Cr micro	10	-	30	Low efficiency
[38]	MWCNT	40	-	~100	High voltage
[14]	Cr/Au micro	20	100 µs	90	High voltage
[41]	Cr/Au micro	10	-	80	Low efficiency
[42]	Cr/Au micro	10	-	80	Low efficiency
[43]	ITO micro	30	-	61	Low efficiency
[44]	Cr/Au micro	5-6	5-10 min.	>95	Longer time
[45]	3D carbon micro	130	400 ms	90	High voltage
[46]	Pt/Ta micro	20	0.5-2 s	~100	High voltage
Our work	**3D Nano spikes**	**2**	**12ms**	**100±0.1**	**Low voltage High efficiency**

TABLE II
COMPARISON OF ELECTRIC CELL LYSIS ON ELECTRODES WITH AND WITHOUT NANOSTRUCTURES

Ref.	Nano-structures	Voltage requirement (V)	Without nano-structures (V)	Efficiency (%)
[38]	MWCNTs	40	85	100
[35]	CNTS	35	135	>95
[36]	CNTs	35	135	>95
[37]	CNTs	40	>90	100
[34]	Nano-gaped ITO electrodes	9	-	~90
this paper	3D Nano-spikes	2	>10	100±0.1

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integration with downstream processes as no lysis agents required [2]–[6], [14]. ECL employs intense pulsed electric field to induce irreversible nanopores on cell membrane which leads to cell lysis [2], [3]. ECL has been proved effective in avoiding complete cell disruption, micronization of cell debris and contaminants from intracellular compartments by selectively lysing the cell membrane rapidly and quickly [15]. Besides these advantages, ECL methods are limited by high energy consumption (5-500 J/mL) and voltage requirement (few tens of volts) as listed in Table 1 to achieve critical electric field for cell lysis E_{CL} (kV/cm). To fulfill these requirements, special costly and bulky power generators are necessary. This is highly undesirable in portable LOC applications [3], [4], [16]. Various designs have been proposed to achieve E_{CL} at low voltages either by decreasing the distance between electrodes or focusing electric field through small constriction segments and structures in microchannels or micro-chambers [2]–[4], [17]. Most commonly used 2D planar electrodes suffer from uneven exposure of cells to an electric field, resulting in low cell lysis efficiencies η_{lysis} [3], [16]. 3D electrodes were designed to overcome this drawback which showed higher η_{lysis} (30%) as compared to 2D electrodes (8%) [18]. However, the fabrication of 3D electrodes usually involves complex, time-consuming and costly fabrication steps [19], [20].

Direct current (DC) voltage is preferred as cell membrane experienced larger transmembrane potential (TMP) without lysing the intracellular components [3], [4], [17]. However, the voltage required to achieve electric field in kV/cm range usually lead to water electrolysis which may lead to gas bubble generation, extreme pH conditions and Joule heating [3], [21]. Alternating current (AC) voltages have been used to minimize these problems for on-chip ECL at optimized frequencies [3], [4], [21]. Depending on applied electric pulse amplitude, duration and number (usually high for ECL), AC ECL techniques also suffer from gas bubble generation, Joule heating, and pH variations [21]–[24]. These undesirable phenomena resulted in the production of unwanted electrolytic chemical compounds led to electrode degradation, effects on thermo-sensitive intracellular contents, i.e., proteins and on reaction kinetics of specific application [25]–[27]. To avoid these drawbacks, subcellular sized constriction structures were employed in a microchannel, so that maximum potential drop was across the cell membrane trapped in these structures instead of in the vicinity of the electrodes [28], [29]. The integration of these structures on portable LOC is limited by complex and costly manufacturing steps, expensive equipment for micro/nanoflow, channel blocking by cell debris and bubbles [3], [17], [25]–[27]. The average electric current between the electrodes can also be reduced by applying AC pulses with low amplitude and shorter duration. However, pulse parameters should be optimized to achieve high η_{lysis} in addition to the minimization of undesirable electrochemical reactions [21], [25], [30], [31]. Cell lysis efficiencies were always a concern in previous reports and η_{lysis} were well below 100% in most of the methods mentioned above [2], [3], [4] (Table 1).

High-aspect-ratio nano-structures (nano-tubes, nano-wires etc.) were incorporated on electrodes to locally enhance electric field intensity to cell membranes and used for cell lysis [32]–[37]. The cell lysing results on these chips indicated that required voltage reduced as compared to electrodes without nano-structures but still in the range of few tens of volts [32]–[37] (Table 2). One of the bottlenecks in the integration of nanostructures on microchips are the difficulties in handling, aligning and positioning the nanostructures at the exact desired location [46]. Furthermore, the fabrication techniques employed are complex, costly, time-consuming and non-reproducible [46]. It is highly desirable to establish simple, inexpensive, reliable and scalable fabrication techniques for fabrication of reproducible and aligned nanostructures to be used in integrated portable LOC systems and potential mass production [9], [46]–[48].

In this work, we present a low-cost 3D nano-spike based electric cell lysis chip which employed self-aligned highly

ordered 3D Aluminum (Al) nano-spike (NSP) arrays fabricated through electrochemical anodization and etching (EA&E) processes using anodic alumina membrane(AAM) as a template. 3D self-aligned highly ordered nano-structures were fabricated using EA&E processes recently due to their simplicity, low cost, reproducibility, and scalability [49]. These nano-structures showed enhanced performance in the field of electronics, optoelectronic, photovoltaic, magnetism, medical, and biology [49], [51]–[54]. Alumina is already recognized as bio-compatible material and used in hip arthroplasty [55], tissue engineering especially for skin replacement [56], bone implant [57], and cell culture and proliferation [58].

We developed an energy-efficient 3D nano-spikes based electric cell lysis (NSP-ECL) chips for efficient cell lysis at low energy consumption. NSP-ECL chips comprised of highly-ordered high-aspect-ratio (λ) 3D Al NSP arrays with controllable dimensions, i.e., length, L_{ns}, base radius, R_{ns}, and pitch, P_{ns} (spike to spike distance). These optimized aspect-ratio λ ($= L_{ns}/R_{ns}$) NSPs were fabricated on low-cost commercial Al foils through simple, scalable, reproducible and cost effective EA&E process. The electric field has been localized at NSPs due to high λ with an enhancement factor α. NSP-ECL chips have achieved high cell lysis efficiencies η_{lysis} (100%) at more than ten times reduced pulse amplitudes (2 V) through localized electric field E_{NSP} as compared to micron-distant parallel plate electric cell lysis (μ PPECL) chips without NSPs. The employment of low-cost EA&E fabrication process, optimized AC electric pulses with low amplitudes (2 V), short durations (few milliseconds) and low energy consumption (0.5-2 mJ/mL) minimized undesirable electrochemical reactions, such as gas and bubble generation on NSP-ECL chips. Due to the scalability of the fabrication process, 3D NSPs were fabricated on small chips as well as on wafers.

II. Nano-spikes Based Electric Cell Lysis System

Schematic diagram of a nano-spikes based electric cell lysis (NSP-ECL) system along with optical micrograph of fabricated nano-spikes on an Al foil and packaged NSP-ECL chip is shown Fig. 1. NSP-ECL chips consist of 3D periodic NSP arrays fabricated on a low-cost commercial Al foil using nano-imprint lithography, electrochemical processes, i.e., anodization and etching and MEMS technology. By controlling dimensions of NSPs, NSPs were fabricated with different aspect ratios λ ($= L_{ns}/R_{ns}$). Large λ resulted in electric field enhancement E_{ns} at NSPs and applied electric field E_a was enhanced with an enhancement factor α. A PCI 6110 DAQ card (National Instrument, TX, USA) and a Labview program were used to apply AC electric pulses with adjustable pulse amplitudes V_a, durations t_p and number P_n to NSP-ECL chips. An Olympus IX70 inverted fluorescent microscope, and a QImaging Retiga 1300C digital CCD camera (Burnaby, B.C., Canada) were used to acquire a set of bright field and fluorescent micrographs before and after ECL through an image capture card. Cell lysis efficiency η_{lysis} were determined as functions of electric pulse parameters (V_a, t_p and P_n) and NSPs dimensions using these acquired images through image processing. Due to E_{ns} and optimized

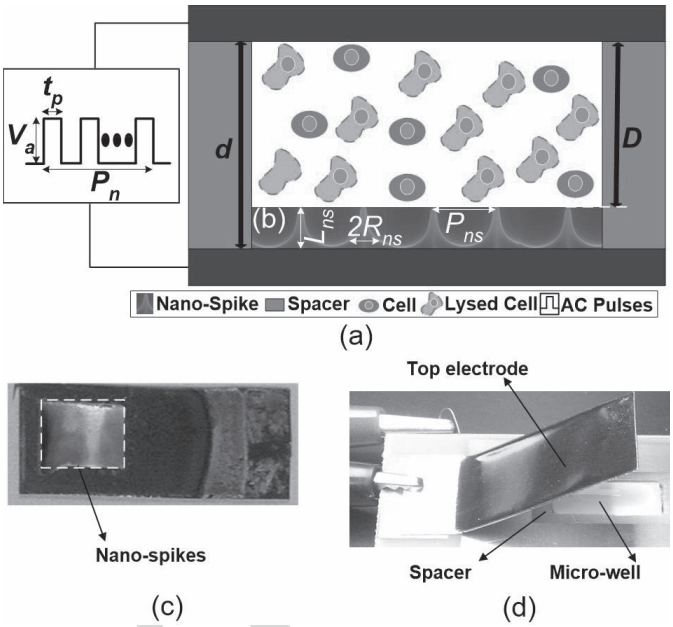

Fig. 1. Illustration of a Nano-Spikes Electric Cell Lysis (NSP-ECL) device, (a) the schematic diagram of an NSP-ECL chip with NSP arrays, (b) SEM micrograph of an array of nano-spikes, (c) optical micrograph of an Al foil with fabricated nano-spikes, and (d) optical micrograph of packaged NSP-ECL chip.

electric pulse parameters, NSP-ECL chips offer the advantage of achieving high η_{lysis} at reduced pulse amplitudes and shorter pulse durations. ECL with low pulse amplitudes and shorter pulse durations minimized undesirable electrochemical reactions such as gas and bubble generation and avoided complete disruption and micronization of cell membrane which is desirable in downstream process integration on LOC system.

A. Nano-Spikes Based Electric Cell Lysis Chip Design

3D periodic NSP arrays on a microchip were fabricated through electrochemical anodization and etching processes. 3D NSPs were fabricated with different controllable dimensions, such as length, L_{ns}, base radius, R_{ns}, and pitch, P_{ns}(spike to spike distance). The top and bottom electrodes are insulated by a spacer (3M Orange Polyimide electrical insulation tape) with a thickness d ($= 100\mu$m). The distance between the tip of the NSPs and the counter electrode of the NSP-ECL chip is defined as D ($= d - L_{ns}$). This spacer not only insulated two electrodes, but also formed a micro-well between two electrodes for cell sample and molecules injection (Fig. 1(a)). The incorporation of optimized aspect-ratio λ NSPs resulted in enhancement of applied electric field. The electric field at NSPs E_{ns} was enhanced by enhancement factor α which depends on the aspect ratio of NSPs. The top electrode of NSP-ECL chip is removable, and cell lysate can be collected from micro-well after electric cell lysis using a pipette.

B. 3D Nano-Spikes Fabrication Process

Major steps involved in the fabrication of NSP-ECL chips were nano-imprinting and scalable electrochemical anodization and etching processes [31], [51]–[54], [59]. First of all, low-cost commercially available *ca* 250 μm thick

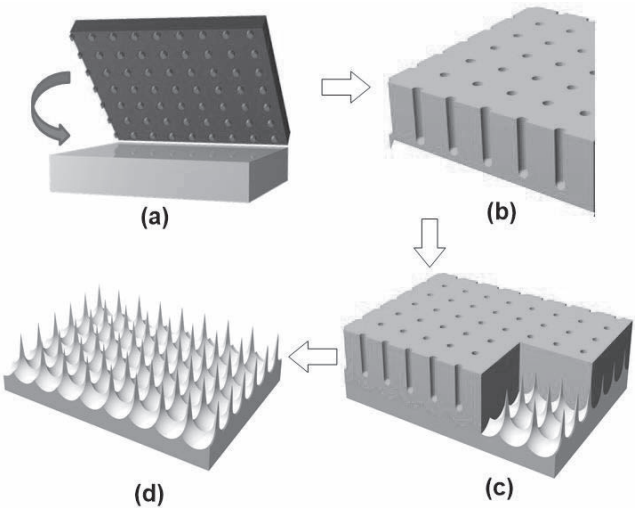

Fig. 2. Key fabrication processes of low-cost highly-ordered 3D nano-spike arrays using electrochemical anodization and etching processes, (a) Al foil was imprinted by a silicon mold with squarely patterned pillars, (b) imprinted Al foil with periodic nanoholes, (c) imprinted substrate was anodized and then etched to fabricate 3D nano-spike arrays, and (d) 3D high aspect-ratio nano-spike arrays fabricated through electrochemical anodization and etching processes.

Al foils (99.99% Alfa Aesar, MA, USA) were cut into pieces of 2×1 cm^2. These Al substrates were cleaned with acetone and then rinsed with isopropyl alcohol and deionized (DI) water. These cleaned substrates were electrochemically polished for 4 minutes at 5°C in a 1:3 (v:v) mixture of perchloric acid and ethanol. A silicon stamp with squarely patterned pillars with a height of ∼200 nm, the diameter of ∼200-500 nm and pitch of 1.2 μm was used for nano-imprinting (Fig. 2(a)). The electropolished substrates were imprinted by the stamp and substrates had perfect squarely ordered nano-indentation which defined the location of the anodic alumina membrane (AAM) pores (Fig. 2(b)). The imprinted substrates were then anodized in a home-built anodization setup using carbon rod as counter electrode using DC voltage of 600 V. The composition of electrolyte used for anodization was 1:1 (v:v) 2wt% Citric acid: Ethylene Glycol + 9 mL 0.1wt% Phosphoric acid. NSPs with different aspect ratios were fabricated by controlling anodization conditions, i.e.; anodization time varies between 30-360 minutes at 10°C. Stability of electrolyte was improved by mixing citric acid with ethylene glycol, and the anodization voltage was increased up to 600 V [51]–[54]. The mixture of phosphoric acid (6%) and chromic acid (1.5%) was used to etch the anodized AAM layer at 100°C for 25 minutes to obtain perfectly ordered 3D NSP arrays (Fig. 2(c)). After etching, the 3D Al NSP electrodes were rinsed with DI water and blown dry with compressed air.

C. Scalability of Nano-Spikes Fabrication Process

The dimensions of NSPs were precisely controlled by controlling the parameters and conditions of EA&E process, i.e., the thickness of AAM, anodization time, etc. NSPs with different lengths L_{ns} ranging from 350-1100 nm was fabricated by increasing anodization time from 30-360 minutes. The maximum achievable L_{ns} was about ∼1100 nm after

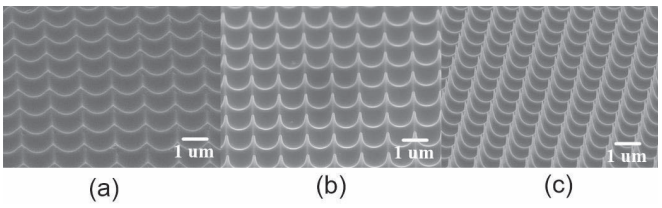

Fig. 3. SEM micrograph of 3D nano-spike arrays with different lengths L_{ns} of (a) 350 nm, (b) 750 nm, and (c) 1100 nm.

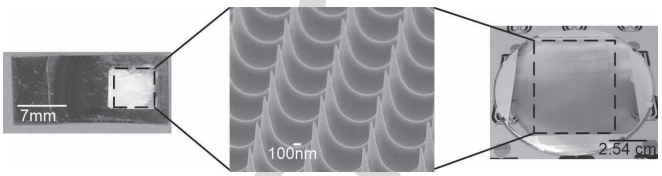

Fig. 4. Highly-ordered 3D nano-spike arrays fabricated on low-cost commercial Aluminum foil with an area of 7mm^2 and also on a 4-inch glass wafer.

anodization of 360 minutes. SEM images of NSP array electrodes with L_{ns} of 350, 750, and 1100 nm with pitch P_{ns} of 1.2 μm are shown in Fig. 3. Several advantages are associated with NSPs fabricated using EA&E processes such as periodicity, self-organization, scalability, reproducibility, and high-aspect-ratio λ. Due to the scalability of above mentioned EA&E fabrication process, it was possible to fabricate NSPs on low-cost Al foils for microchips as well as on 4-inch glass wafers (Fig. 4). The sample in microliter range was processed on 3D NSP-ECL chips, while throughput can be scaled up to handle large cell populations ($10^4 - 10^5$) on NSP-ECL wafers. This simple, low-cost, scalable, reproducible and reliable process is highly attractive for low energy and cost-effective portable μ -TAS, LOC and smartphone-based systems as well as for high throughput and large population applications.

III. Material and Methods

A. Cell Line Preparations

Human cervical cancer (HeLa) cell line was used in the ECL experiments to characterize cell lysis efficiencies η_{lysis} on NSP-ECL chips. HeLa cells were cultured and grown in Eagle's minimal essential medium (EMEM) (CCL-2™, ATCC, VA, USA), supplemented with 10% fetal bovine serum (FBS) (ATCC, VA, USA) and 1% Streptomycin/Penicillin (GIBCO®, Invitrogen Inc., USA) at 37°C and 5% CO_2. To perform the ECL experiments on the NSP-ECL chips, HeLa cells were re-suspended in the Phosphate buffered saline (PBS). Then, the EMEM medium was sucked, washed twice with PBS and trypsinized by 0.25% trypsin/EDTA (GIBCO®, Invitrogen Inc., USA) for 3-5 minutes at 37 °C. The detached cells were centrifuged at 1,200 rpm at room temperature for 3 minutes. The concentration of HeLa cells was adjusted to 1×10^5 cells/mL in suspension.

B. Dual Acridine Orange/Ethidium Bromide Fluorescent Staining

Cell lysis efficiencies η_{lysis} is defined as the percentage of dead cells after application of a lysing electric field [44].

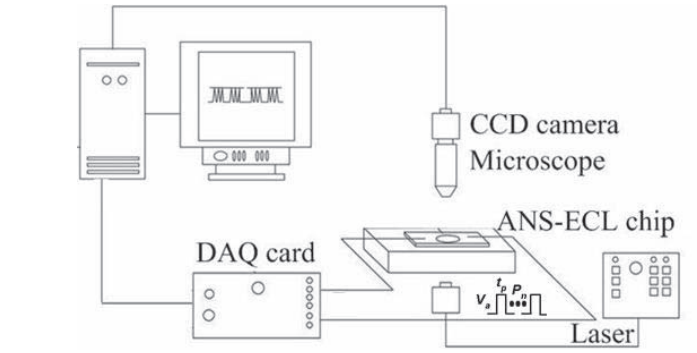

Fig. 5. The schematics of the experimental setup to perform the electric cell lysing on the fabricated NSP-ECL chips.

η_{lysis} can be determined by using dual fluorescent dye staining using Acridine Orange and Ethidium Bromide (AO/EB; Sigma, St Louis, MO, USA) which are nuclear staining dyes [60]–[62]. Acridine Orange (AO) is a membrane permeable dye and emits green fluorescence while Ethidium Bromide (EB) is membrane-impermeable dye and emits red fluorescence after entering the cell through compromised membranes. Upon staining cells with dual AO/EB dyes, live cells emit green fluorescence while lysed cells with damaged membrane emit orange-yellow fluorescence [60]–[62]. To determine η_{lysis}, the cell suspension was injected to the NSP-ECL chips and the electric pulses were applied. False readings from the reversibly electroporated cells were avoided by adding dual AO/EB staining solution to the cell suspension 5 minutes after the application of electric pulses on the NSP-ECL chips. Lysed cells exhibited orange-yellow fluorescence when EB dye bind with DNA/RNA either inside or outside the cell through the ruptured cell membrane. η_{lysis} was calculated by counting cells that appeared orange-yellow under fluorescence over the entire cells.

C. Experimental Setup

A PCI 6110 DAQ card (National Instrument, TX, USA) and a Labview program were used to apply electric pulses with adjustable pulse amplitude (V_a), pulse duration (t_p) and pulse number (P_n) to the NSP-ECL chip as shown in Fig. 5. The cell's response before and after ECL was observed using an Olympus IX70 inverted fluorescent microscope and a QImaging Retiga 1300C digital CCD camera (Burnaby, B.C., Canada) (Fig. 5). Sets of bright field and fluorescence micrographs were acquired by an image capture card. These digital images were processed to determine the η_{lysis} as a function of electric pulse parameters on NSP-ECL chips.

D. Statistical Analysis

At least 100 cells were analyzed to obtain each data point, and each experiment was repeated at least three times. The standard deviation between repeated experiments was shown as error bars.

IV. Electric Field Enhancement

Electric field distribution was simulated to evaluate the electric field enhancement at NSPs. A commercial finite element method (FEM) package (COMSOL Multiphysics 4.2, COMSOL Ltd., USA) was used for electric field distribution simulations [63]. The profile of NSPs was extracted with the help of extract profiles tool using the AFM images of NSPs. The extracted coordinates of NSPs were then exported to COMSOL. The cell lysis chamber is *ca* 100 μm high (the distance between the top and bottom electrode). The top electrode and the tip of the spikes on the bottom electrode were separated by a distance D (99 μm) and the space between the two electrodes was considered as cell suspension medium (Fig. 6). The relative permittivity and conductivity of cell suspension medium were assumed to be 77.4 $\pm$ 5% and 1.7 S/m $\pm$ 10%, respectively [59]. The fixed potential between the electrodes was used as the boundary condition. The fixed potential between the electrodes was applied by selecting 2D stationary electrostatics physics in COMSOL. These simulations demonstrated that applied electric field E_a is enhanced and defined by enhancement factor α which on the other hand highly depend on the aspect ratio λ of NSPs. The enhanced electric field E_{ns} is very large near tips of NSPs and E_{ns} become uniform few nm above 3D NSP arrays as shown in Fig. 6.

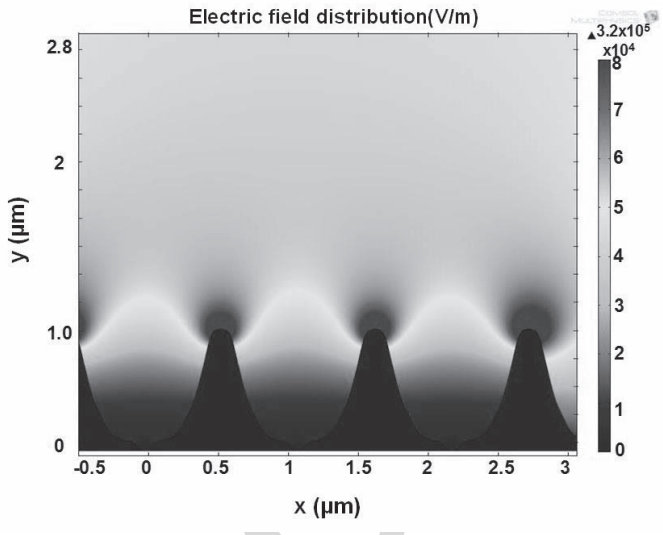

Fig. 6. Numerical simulation of the electric field distribution between nano-spike array electrodes using COMSOL at $V_a = 4$V. The simulation shows local electric field enhancement, especially near the nano-spikes.

The enhanced electric field E_{ns} was localized on NSPs due to the optimized aspect ratioλ of NSPs. The enhancement factor α by which the applied electric field E_a is enhanced can be estimated using the following relation [64], [65]:

$$E_{ns} = E_a \times \alpha \times \gamma \quad (1)$$

where E_a is the applied electric field (V_a/D), α is the enhancement factor and γ is the correction factor to incorporate the electrochemical impedance near the fluid-electrode interface and determined through electrochemical impedance spectroscopy [66], [67]. Based on the geometries of nanostructures, several models have been proposed to estimate α [65]. In our case, the α was estimated by considering NSP as a hemi-ellipsoid with length L_{ns} and base radius R_{ns} as

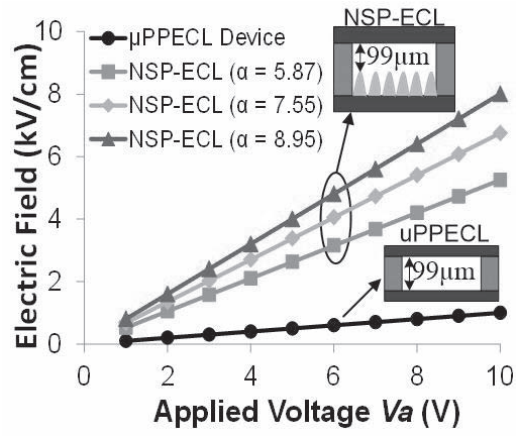

Fig. 7. Electric field as a function of applied voltages V_a for micro parallel plate electric cell lysing (μ PPECL) device without nano-spikes and NSP-ECL devices with different α.

follows [65]:

$$\alpha = \xi^3/[\{\lambda ln(\lambda + \xi)\} - \xi] \quad (2)$$

where $\xi = (\lambda^2 - 1)^{1/2}$ and λ is the aspect ratio of NSP (L_{ns}/R_{ns}). It is evident from (2) that α is a function of λ and α can increase exponentially with increasing λ. λ. As mentioned previously, the aspect ratio λ can be controlled by controlling dimensions of NSPs. We have successfully fabricated NSPs with λ up to 3 using EA&E process. For NSPs with L_{ns} of 1100nm, the R_{ns} was 375nm which leads to the aspect ratio of around 3. For NSPs with λ ranging between 2 and 3, α was estimated between 5.9 and 8.9 using Equation (2). For micron-distant parallel plate electric cell lysis (μ PPECL) devices without NSPs, the electric field E_{planar} can be estimated as the ratio of applied voltage V_a to the distance between parallel plate electrodes $D(E_{planar} = V_a/D)$. Interelectrode distance D of ~99 μm was considered for both μ PPECL and NSP-ECL devices to compare electric field. Enhanced electric field at NSPs E_{ns} was determined using (1) and (2). The electric field was enhanced at NSP-ECL devices by enhancement factor α as compare to μ PPECL devices (Fig. 7). This means that lower voltages are required to achieve a specific electric field on the NSP-ECL devices depending on α as compared to μ PPECL devices. For example, electric field of 2 kV/cm can be achieved at 20 V for μ PPECL device, at ~4 V for NSP- ECL device with α of 5.87, at ~3 V for NSP- ECL device with α of 7.55 and at ~2.6 V for the NSP-EP ECL device with α of 8.95 (Fig. 7).

V. Results and Discussion

When a cell is exposed to an externally applied electric field, localized transient microstructural changes and nanopore generation takes place in the cell membrane. These changes and induced nano-pores can either resealed (reversible electroporation) or non-resealed (irreversible electroporation) depending on applied electric pulse parameters V_a, t_P and P_n [34]–[37]. Irreversible electroporation causes rupturing of the cell membrane and cell lysis due to dielectric breakdown of the cell membrane as cell unable to maintain essential ionic balance across the membrane. ECL occurs only when applied electric pulse parameters V_a, t_P and P_n are well above their critical values [4]. Irreversible nano-pore generation is initiated when an electric field is well above its critical value E_{CL} which in turn determined by pulse amplitude V_a and density and duration of these nanopores depend on t_P and P_n [34]–[37]. It is critical to optimize these electric pulse parameters to achieve high η_{lysis} at low energy consumption to avoid undesirable electrochemical reactions and possible integration with portable devices. In our ECL experiments, we have applied rectangular AC pulses with adjustable V_a of 1–10 V, t_P of 1–12 ms and P_n of 1-10 on NSP-ECL chips with α of 5.87, 7.55 and 8.95.

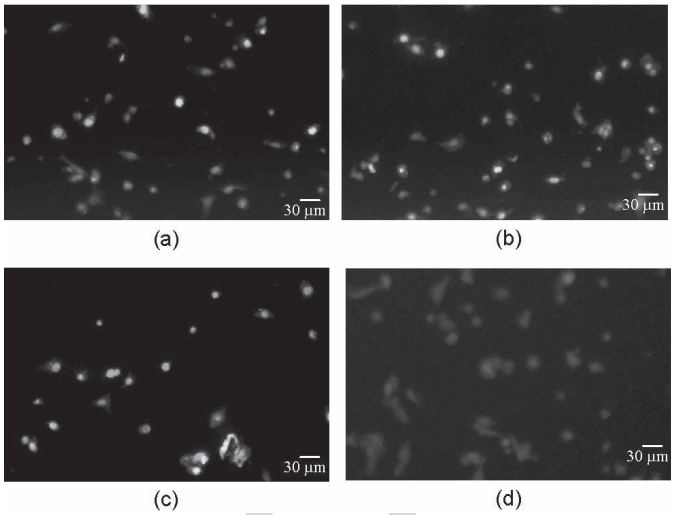

Fig. 8. Fluorescence micrographs of Acridine orange and Ethidium bromide dual stained HeLa cells treated on NSP-ECL chips and μ PPECL devices. Viable cells exhibit green fluorescence while lysed cells exhibit orange-red fluorescence due to loss of membrane integrity. (a) HeLa cells undergone electric cell lysis (ECL) on μ PPECL without nano-spikes at pulse amplitude $V_a = 5$V and pulse duration $t_P = 12$ms, (b) HeLa cells before ECL on NSP-ECL chips ($\alpha = 8.9$), (c) HeLa cells after ECL on NSP-ECL chips ($\alpha = 8.9$) at $V_a = 2$V and $t_P = 10$ms, and (d) HeLa cells after ECL on NSP-ECL chips ($\alpha = 8.9$) at $V_a = 2$V and $t_P = 12$ms.

A. Fluorescence Microscopy

Cell lysis efficiencies were quantified by using dual AO/EB fluorescent staining (Fig. 8). Fluorescence micrographs of cells before ECL on NSP-ECL chips showed no yellow-orange fluorescence as cell membrane was intact and impermeable to EB dye molecules (Fig. 8(b)). After ECL, cell membrane ruptured due to induction of irreversible nanopores on cell membranes by applied electric field. EB molecules entered the cells through compromised membrane and stained the lysed cells. Lysed cells exhibited orange-red fluorescence, while the live cells emitted green fluorescence (Fig. 8(c) & (d)). Almost all cells exhibited orange-red fluorescence when lysed on NSP-ECL chips at 2 V and 12 ms pulses showing high η_{lysis}. Fluorescence micrograph of ECL on μ PPECL devices at 5 V and 12 ms pulses showed almost no orange-red fluorescence showing very low η_{lysis} (Fig. 8(a)).

B. Enhancement Factor Effect on Electric Cell Lysis

Cell lysis efficiencies were quantified on NSP-ECL chips with different α and on μ PPECL devices in order to determine

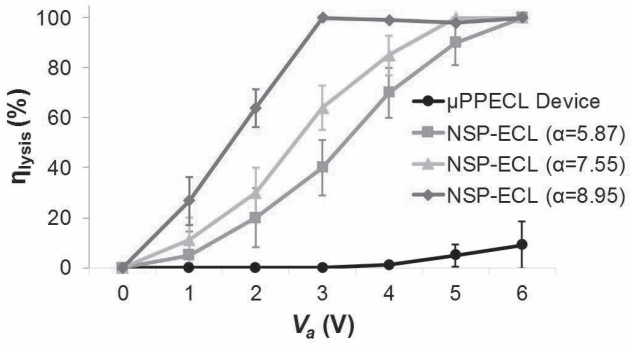

Fig. 9. Cell lysis efficiency η_{lysis} as a function of applied pulse amplitude V_a on NSP-ECL chips with different α (5.9, 7.5, 8.9) and the cell lysis efficiency of the μ PPECL device for pulse duration t_P of 10ms.

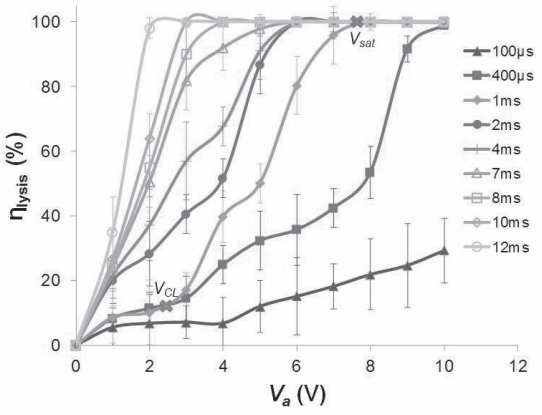

Fig. 10. Cell lysis efficiency η_{lysis} as a function of V_a and t_P for P_n of 10 on NSP-ECL chip.

the effect of α on η_{lysis} as compared to μ PPECL devices without NSPs. From Fig. 9, it is clear that cell lysis on NSP-ECL chips showed higher η_{lysis} as compared to cell lysis on μ PPECL devices at specific V_a due to enhanced electric field E_{ns} on NSPs. At $V_a = 3$ V, the η_{lysis} was 40 to 100% high on NSP-ECL chips as compared to μ PPECL devices depending on enhancement factor $\alpha$of NSP-ECL chips. η_{lysis} was increased with increasing α on NSP-ECL chips at specific V_a. η_{lysis} of 40%, 64% and 100% were achieved at $V_a = 3$ V on NSP-ECL chips with α of 5.87, 7.55 and 8.95 respectively. NSP-ECL chips with α of 8.95 was selected for further analysis due to high η_{lysis} at low voltages.

C. Critical Values for Electric Cell Lysis

Based on the applied electric field, ECL process can be divided into three phases as shown in Fig. 10. When the applied electric field is below critical electric field E_{CL}, η_{lysis} is very low as the electric field is not sufficient to induce enough irreversible nano-pores rather reversible nanopores on the cell membrane. When the applied electric field was above E_{CL}, the electric field was strong enough to break down the integrity of cell membrane by inducing enough irreversible nano-pores. EB fluorescent molecules bound to DNA/RNA inside or outside the ruptured cell membrane and lysed cells exhibited orange-red fluorescence (Fig. 8(c) and (d)). At this stage, a small increase in pulse amplitude V_a, more and more cells lysed and η_{lysis} increased quickly (Fig. 10). η_{lysis}keep on increasing by increasing electric field until η_{lysis} saturated and electric field at this point defined as saturation electric field E_{sat}(Fig. 10). Further increase in V_a did not improve η_{lysis} but increased power consumption.

D. Electric Pulse Parameters Effects on Electric Cell Lysis

The cell lysis efficiencies were greatly influenced by applied electric pulse parameters such as V_a, t_P and P_n. Higher η_{lysis} can be achieved at higher pulse amplitude V_a, longer pulse duration t_p and higher pulse number P_n(Fig. 10). Higher pulse amplitude V_a and longer pulse duration t_p increased power requirement and may also induce undesirable electrochemical reactions. Electric pulse parameters should be optimized to achieve high η_{lysis} but at lower V_a and shorter $t_p$to minimize electrochemical reactions and power requirement. We have reached high η_{lysis}(∼100%) at V_a of 2 V, t_p of 12 ms and P_n of 10 on NSP-ECL chip (Fig. 10). This reduction in V_a is more than ten times lower as compared to μ PPECL devices.

E. Energy Requirement for Electric Cell Lysis

The energy consumption for electric cell lysis is a crucial issue especially in LOC, μ -TAS and smartphone based microsystems where limited energy is available [3], [68]. This energy requirement is high enough to employ complex, bulky and costly power generators and equipment [16], [69]. Due to high energy requirement, ECL systems usually undergo metal ion dissolution, local pH variation, Joule heating, gas and bubble generation and sample contamination [3], [4], [5], [17], [25], [68], [70]. In order to avoid these undesirable reactions on ECL devices and to integrate them on LOC, μ-TAS and smartphone based microsystems; low energy consumption ECL systems are highly desirable. In our approach, we utilized 3D nano-spikes on which electric field was enhanced due to their optimized aspect-ratio. We were able to achieve cell lysis at lower pulse amplitudes due to electric field enhancement. The specific energy input W delivered to samples on NSP-ECL chips was calculated using relation:

$$W = V_a I P_n t_p / vol \quad (3)$$

where V_a is the applied pulse amplitude, I is the electric current, P_n is the pulse number, t_p is the pulse duration, and *vol* is the sample volume (0.25 mL). A high-precision 1kΩ resistor was connected in series with the chip and serve as the current-to-voltage converter. The resistance of the resistor is too small as compared to the chip. Therefore, it can be ignored in the electric current calculation. The voltage signals from this resistor were measured by using a PCI 6110 DAQ card (National Instrument, TX, USA) and a Labview program and used in the electric current calculation. The specific energy input W required to achieve optimized electric pulse protocol (2V × 12ms for 10 pulses) was 0.5 mJ/mL (Fig. 11). The energy consumption for cell lysis on NSP-ECL

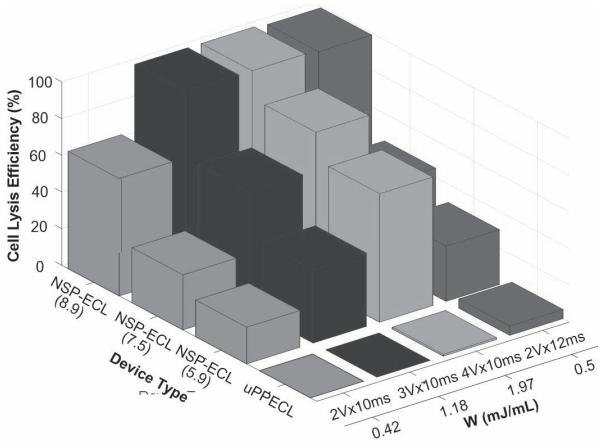

Fig. 11. η_{lysis} for different NSP-ECL and μ PPECL devices as a function of different electric pulse protocols and specific energy input W (mJ/mL).

TABLE III
SPECIFIC ENERGY REQUIREMENT FOR CELL LYSIS USING DIFFERENT METHODS

Ref.	Methods	Device characteristics	Treatment time	Specific energy input
[72]	Laser	Beam dia. of 100µm	60sec × 10 times	16kJ/mL
[72]	Microwave	1025W 2.45GHz	20min.	74.6kJ/mL
[72]	Mechanical solid shear	Blade dia. 40mm 120W, 3000 rpm	6min.	540kJ/mL
[72]	Thermal lysis	90^0C	20min.	20.1 kJ/mL
[72]	Liquid shear ultrasonication	40W ultrasonic bath	20min.	132 kJ/mL
[73]	High voltage pulsed electric field	$L\times W$=30×3mm^2 d = 10mm	1µs	100-200 J/mL
[74]	Electroporation	A=0.78cm^2 d = 0.3cm	µs-ms	16-150 J/mL
[75]		$L\times W$:2.8×0.6cm^2 d = 1mm	100µs × 32	5-533 J/mL
This paper	NSP-ECL device	NSP dimensions L: 350-1100nm D: 200-500nm	12ms × 10	0.05-3 mJ/mL

$L\times W$: electrode length × width, d: interelectrode distance, A: electrode area, D: diameter

chips was 0.5-2 mJ/mL that is 3-9 orders of magnitude lower as compared to other cell disintegration methods as shown in Table 3.

Low device reliability and failure were observed in macro and micro ECL devices due to high voltage operations which resulted in electrolysis, gas bubble generation, Joule heating, local pH variations, etc. [21]–[27]. Electrode degradation and cell damage were observed during electroporation and ECL processes due to gas bubbles generation which resulted in local pH variations and violent hydrodynamic forces [21]–[24], [59]. Gas bubble generation was observed on micro devices due to high voltage operation especially above 6 V [22], [75] as shown in Fig. 12(b). Although AC pulses were applied on micro devices which were known to minimize electrochemical reactions, still applied pulse amplitudes were high

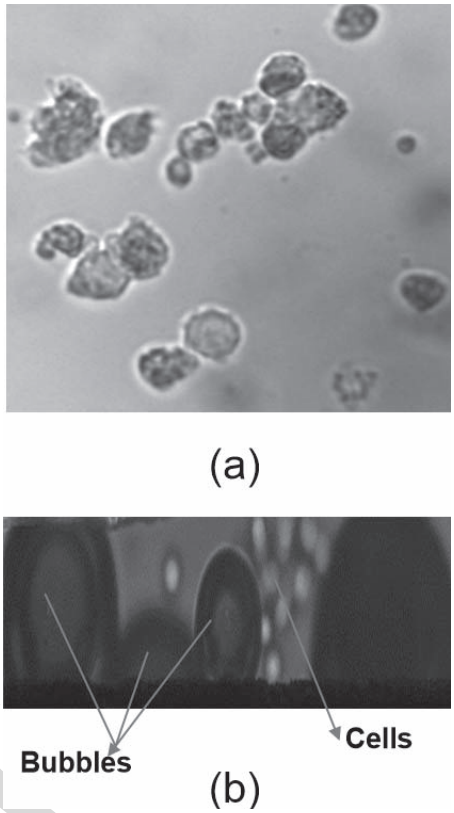

Fig. 12. Cell morphologies after electric cell lysis on (a) NSP-ECL chips, bubble generation, and cell micronization was avoided and (b) on a micro ECL chip, Bubble generation was observed on micro devices [22], [75].

enough to induce gas bubble generation and electrode degradation (Fig. 12 (b)). On the other hand, on NSP-ECL chips, due to the employment of NSPs, high η_{lysis} was achieved at low pulse amplitudes without bubble generation (Fig. 12(a)). In addition, the cell membrane was not fully disintegrated after ECL on NSP-ECL chips (Fig. 12(a)). This will avoid micronization of cell debris and complex, costly and time-consuming downstream processes.

F. Phase Diagram for Electric Cell Lysis

ECL occurs successfully when applied electric field is well above its critical value E_{CL}. It is crucial to determine electric pulse parameters to achieveE_{CL} as if the electric field is below this critical value; cells will be reversibly electroporated instead of lysed. E_{CL} was achieved at different V_a for different t_p, at lower V_a for longer t_p, and at higher V_a for shorter t_p. E_{CL} is defined as a critical electric field for cell lysis which induces irreversible nanopores on the cell membrane and η_{lysis} increases quickly. We have also determined electric pulse parameters to achieve saturation electric field E_{sat} at which η_{lysis} saturated. It is vital to determine E_{sat} as increasing pulse parameters after this point will only result in additional power hence energy consumption and micronization of cell debris which is not suitable for portable LOC systems and downstream processes. Using these parameters for E_{CL} and E_{sat}, we have constructed "phase diagram" for ECL of HeLa cells on NSP-ECL chips (Fig. 13). Phase diagram defines

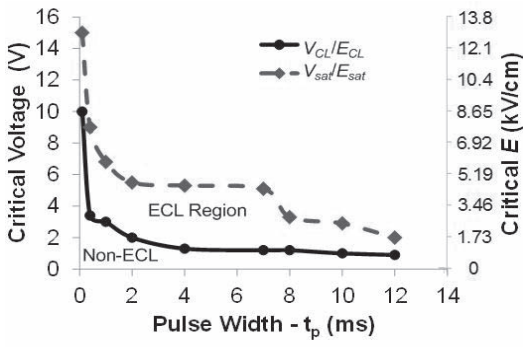

Fig. 13. The Phase diagram for the electric cell lysis of HeLa cells on the NSP-ECL chip ($\alpha = 8.9$). The Phase diagram shows the non-ECL and ECL regions for different applied pulse durations.

the boundary for non-ECL and ECL regions for different electric pulse parameters. Minimum pulse amplitude $V_{CL,min}$ to achieve E_{CL} was 0.9 V for t_p of 12 ms which is more than thirteen times lower as compared to μ PPECL devices. Minimum pulse amplitude $V_{sat,min}$ to achieve E_{sat} was 2 V for t_p of 12 ms which is more than ten times lower as compared to μ PPECL devices.

VI. Conclusion

In conclusion, we have developed a low-cost energy-efficient 3D nano-spike based electric cell lysis (NSP-ECL) chips for efficient cell lysis at low pulse amplitudes and duration. Highly-ordered self-aligned 3D Al NSP arrays with controllable dimensions, i.e., length, L_{ns}, base radius, R_{ns}, and pitch, P_{ns} (spike to spike distance) were fabricated on low-cost commercial Al foils through simple, scalable, reproducible and cost effective electrochemical anodization and etching processes. The electric field has been localized at NSPs due to optimized aspect-ratio with an enhancement factor α as compared to micro-distant parallel plate electric cell lysis (μ PPECL) chips without NSPs. NSP-ECL chips have achieved high cell lysis efficiencies η_{lysis} (100%) at more than ten times reduced pulse amplitudes (2 V) through localized electric field E_{ns} as compared to the μ PPECL chips without NSPs. These applied pulse amplitudes are 2-3 times reduced as compared to traditional electroporation systems used for different applications. The specific energy input required to achieve 100% η_{lysis} was only in the range of 0.5-2 mJ/mL which is 3-9 orders of magnitude lower as compared to other cell disintegration methods (5J/mL-540kJ/mL). The employment of NSPs fabricated through low-cost EA&E process, optimized AC electric pulses with low amplitudes and short durations minimized undesirable electrochemical reactions, such as gas and bubble generation on NSP-ECL chips which were observed on micro devices due to high voltage operation. Due to the scalability of the fabrication process, 3D NSPs were fabricated on small chips as well as on wafers to process samples for microsystems as well as for high throughput applications. These energy-efficient NSP-ECL chips are highly attractive for integration with other sample preparation downstream processes on portable LOC and μ-TAS systems due to its low power consumption, reliability, cost-effectiveness and avoiding micronization of cell debris. Based on these low voltage devices, we can add additional ECL tool in a recently developed "Lab on Smartphone" through which optimized EP protocols can be applied to micro/nano EP chips through an open-source MCU (Arduino) with an integrated Bluetooth module [48].

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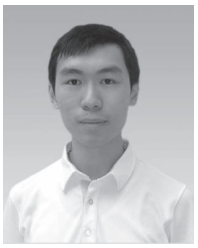

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