

Perovskite-Nanowire-Array-Based Continuous-State Programmable Artificial Synapse for Neuromorphic Computing

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Perovskite-based memristors with tunable nonvolatile states are developed to mimic the synaptic interconnects of biological nervous systems and map neuromorphic computing networks to integrated circuits. To emulate the plasticity of synaptic structures, memristors with robust multilevel resistive states are fabricated in this work using high-density polycrystalline MAPbCl₃ nanowires (NWs) array that vertically integrated using solution method. In particular, the fabricated memristors exhibit both short- and long-term plasticity and traits akin to biological synapses. A fabricated memristor device is precisely programmed to 18 resistive states and each state exhibits stable data retention of more than 100 000 s. Furthermore, a matrix processing unit using a 4-by-4 memristor array is fabricated as the hardware core of an encoder–decoder artificial neural network to demonstrate high accuracy and reliable in-image font conversion. The resistive states of the 16 memristors are precisely programmed to the corresponding resistance values for specific synaptic weights of the artificial-neural-network-trained offline. In addition, experimental characterization and first-principles simulations attribute the continuous programmability and high reliability features of the memristors to the confinement mechanisms of the horizontal grain-boundary structure in polycrystalline perovskite NWs.

1. Introduction

Synaptic structures play a vital role in transmitting neural signals in the central nervous system. The strength or efficacy of synaptic transmission can be modified by neural activity, thereby altering the thinking, feeling, and behavior of organisms.^[1] It is widely believed that memory is encoded by changes in synaptic strength through potentiation and depression of cellular mechanisms.^[2] The neuromorphic computing architectures that simulate the nervous system of the biological brain, such as deep neural networks^[3] and spiking neural networks,^[4] realize the information storage and input preprocessing through the synaptic connections with continuously programmable conductivities. Memristors have emerged as key components for artificial synapses in neuromorphic computing hardware.^[5–7]

To realize efficient information storage, memristors with continuously programmable resistive states that mimic the plasticity

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of biological synapses are essential. The resistive state of the memristor is the result of the previous energy input, modified by the mechanism of conductive filament (CF) formation and rupture.^[8] Specifically, memristors operating in the valence-change mechanism (VCM) use vacancy-based CFs, where vacancies conduct current by locally doping the material, while the valence ions accumulate near the anode, allowing continuous-resistive-state changes during device set and reset.^[9,10]

Organic-inorganic hybrid perovskite materials with ABX₃ structures exhibiting innate hysteresis and high mobility properties have been used as switching layers for VCM-based memristors to realize artificial synaptic devices.^[11–15] Solvent engineering offers a convenient method for modifying the crystal structure and elemental composition of perovskite materials, facilitating device optimization and large-scale fabrication on solid or flexible substrates.^[15] To address challenges such as vulnerability of perovskites to ambient environment and the instability of lateral electrical leakages,^[16–18] we have developed reliable memristors structure by incorporating porous alumina membrane (PAM) template encapsulated perovskite NWs as switching layers.^[19–21] However, achieving controllable multi-level resistive states and long retention performance in perovskite memristors remains a key challenge.^[22]

Several experimental approaches have demonstrated the multi-level programmability of memristors using the device anode as a reservoir to absorb valence ions. However, these methods often compromise device retention and durability.^[23,24] The resistive switching layer, with its high concentration of charged vacancies and ions, can exhibit drastic changes in filament conductivity to a small fluctuation in the distribution of mobile charges.^[10,25,26] Consequently, precise regulation of the memristor-resistive states often demands complex control circuits and algorithms to provide specific compliance current levels.^[27,28] Further research indicated that the local heating effect near the main CF of the memristor makes it difficult to control the resistive states precisely and stably.^[29,30] It has been reported that memristors adopt a multilayer structure including ion reservoir layers and barrier layers can achieve precise and stable control of the resistive states, thereby programming the resistive states more precisely and improving retention stability.^[31,32]

In this article, we present the design of a solution-process-synthesized polycrystalline perovskite nanowires (NW) array to fabricate memristors with stable and continuously programmable resistive states. The polycrystalline nanostructure of perovskite materials effectively confines the transport of charged mobile ions through grain boundaries (GBs) can enhance CF stability.^[33–35] Solvent engineering has been adopted to fabricate the NWs array within the PAM template. Furthermore, we fabricated a computational core integrated using precisely programmed memristor matrix to replace one computational layer of an artificial neural network (ANN) for in-image font conversion. Finally, a plausible working principle of the memristor is suggested based on the first-principles simulations.

2. Result and Discussion

In biological synapses, the synaptic weight is determined by the amount and species of neurotransmitters received by the

neuro-receptors on the cell membrane of the post-synaptic terminal.^[36–38] As illustrated in **Figure 1a**, the synapse with a higher conductivity has more neuro-receptors on the post-synaptic cell membrane, and more neuro-transmitter can be released through the presynaptic terminal. The synaptic conductance can be enhanced or weakened by electrical stimuli, termed potentiation and inhibition processes in neuroscience.^[38] Such a dynamic conductance feature of the biological synapse can be mimicked using the MAPbCl₃-NWs-array-based memristors.

As shown in **Figure 1b**, the memristor is composed of an aluminum (Al) cathode electrode, a top indium-zinc-oxide (IZO) anode, and the switching layer of MAPbCl₃ NW array assembled in the PAM template. A cross-sectional scanning transmission electron microscopy (STEM) image of the MAPbCl₃ NWs is shown in **Figure 1c**, which are ≈70 nm in height and ≈15 nm in diameter. In addition, the energy-dispersive X-ray (EDX) mapping shown in **Figure S1**, Supporting Information, depicts the elemental distribution. Such a small area of a single NW facilitates the downscaling of memristors.^[19] The X-ray diffraction (XRD) pattern shown in **Figure 1d** suggests that the grains have a standard cubic MAPbCl₃ crystal structure with a predominant (100) orientation,^[39] confirming the successful fabrication of MAPbCl₃ NWs.

Figure 1e exhibits the typical current–voltage (*I*–*V*) characteristics of the IZO/MAPbCl₃/Al-structured memristor. The device shows a smooth and gradual *I*–*V* curve of SET/RESET process under a dc voltage sweep of 0 V → +3 V → 0 V → –2 V → 0 V, allowing the resistive states of the memristor to be continuously programmed. To demonstrate the typical resistance regulation feature of memristors, **Figure 1f** shows a gradual conductance increase of a device under 10 consecutive dual-positive DC voltage sweeps (0 V → 3 V → 0 V), emulating the synaptic potentiation process.

In the biological nervous system, neural signals are encoded into electrical pulses with a variety of durations, magnitudes, intervals, and frequencies.^[40,41] These spiking neural signals cause short- (STP) and long-term plasticity (LTP) of the synapses, which are thought to underlie learning, forgetting, and memory. Here, we show that MAPbCl₃-NWs-based memristors fabricated in this work can respond to electrical stimuli with distinct patterns and exhibit both STP and LTP.

Figure 2a shows the STP of our MAPbCl₃-NWs-array-based memristor. The memristor was initially reset to a high-resistive state (HRS) and then excited to lower resistances using square pulses with 1 V amplitude, 10 s pulse interval, and duration of 20 and 50 ms. The conductive states of the memristor were monitored by a DC bias voltage of 0.1 V. The timing of excitation and monitoring periods of the test signal is illustrated, and the device resistance is indicated by the readout current in the monitoring period. The results show that the device resistance is reduced right after the excitation pulse and then slowly increases to higher-resistive states. Particularly, the excitation pulse with a longer duration results in lower device resistances, showing an efficient response of the device resistive state to the duration of the excitation signal.

Further, we characterized the response of memristor-resistive states to the excitation signal amplitudes. As shown in **Figure 2b**, the excitation-pulsed signals with 2.5 and 0.5 V in amplitude (50 ms duration and 10 s interval) were applied. The memristor

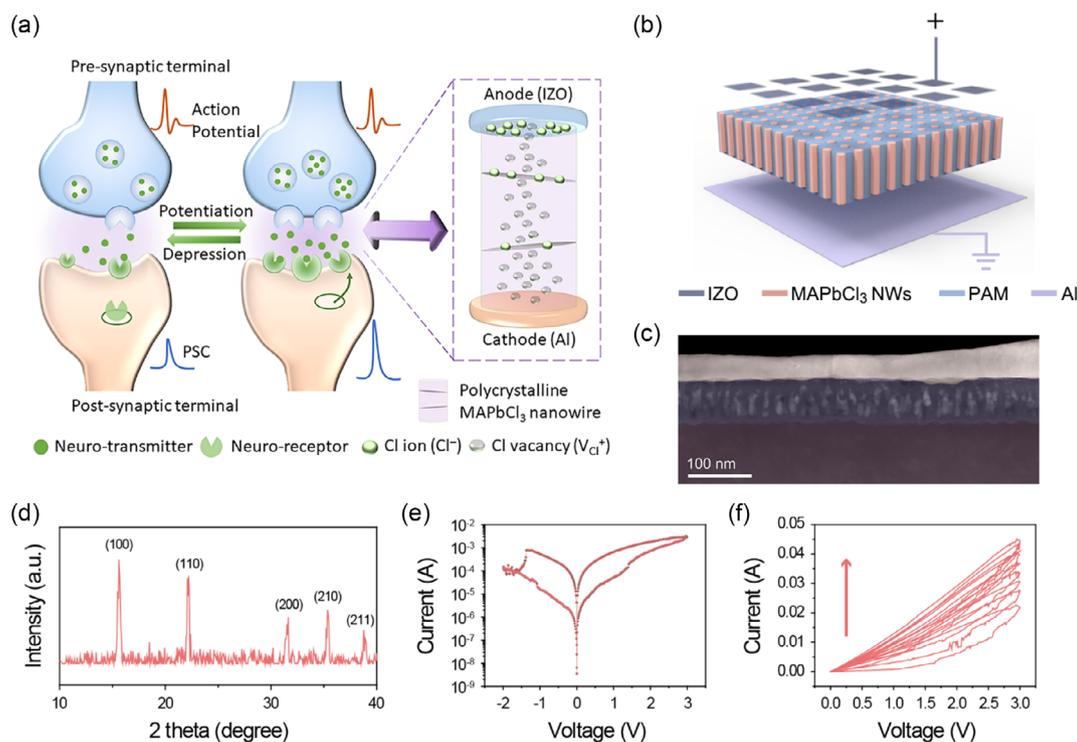


Figure 1. Device structure and basic electrical characteristics. a) Schematic demonstration of synapse structure and the sketch of the artificial synapse device. b) Device schematic of MAPbCl₃ NWs in the PAM template with IZO as the top electrode and Al as the bottom electrode. c) Cross-sectional STEM of MAPbCl₃ NWs in PAM. d) XRD characterization of MAPbCl₃ NWs (arbitrary units [a.u.]). e) Typical *I*–*V* characteristics of IZO/MAPbCl₃ NWs/Al memristor. f) *I*–*V* curves under 10 consecutive dual-positive-voltage sweeps.

shows the typical STP characteristics to both of the excitation signals. Meanwhile, the signal with 2.5 V amplitude causes the memristor to exhibit synaptic potentiation features with an STP mechanism.

As shown in the left plot of Figure 2c, we applied the excitation pulses for 20 times to amplify the effect. We found that the trend of reducing device resistance emulates the learning and forgetting of the Ebbinghaus curve. Moreover, the synaptic potentiation induced by excitation signals of different amplitudes is compared. As shown in the right plot of Figure 2c, the potentiation effect is indicated by the ratio of device readout current measured after the 10th excitation over that measured after the 1st excitation. The results show that the excitation signal amplitude has a super-linear effect on synaptic potentiation.

In addition, the device exhibits significantly different responses to excitation signal frequencies, a feature of learning and forgetting in the STP mechanism. As shown in Figure 2d, the memristor shows a sustained decrease in resistance driven by a 1 V excitation-pulsed signal with a 1 s interval and 50 ms duration. In contrast, the signal with 10 s interval shows no such effect on regulating the device resistance.

Complementary to synaptic potentiation, synaptic depression adds flexibility in regulating neural network interconnections. The synaptic depression characteristics of the memristor were measured with –1 V inhibition-pulsed signals with various durations and intervals. The results plotted in Figure 2e,f show that the device can effectively realize the synaptic depression behavior

with STP characteristics and shows more obvious depression with a shorter pulse interval (≤ 2 s).

Repeated stimulation has realized LTP in the MAPbCl₃-NW-array-based memristors. After the device has been set to a relatively low-resistive state, Figure 2g shows the long-term potentiation and depression process of the memristor mimicking synaptic behavior. As illustrated by the testing scheme, the potentiation and depression processes were simulated using +1 and –1 V pulsed signals, respectively, and 1000 stimulation pulses were applied for each process. The plotted device readout current was measured using 0.1 V pulsed signals after each stimulus. The results show that the change of device-resistive state gradually decreases with the increase in the number of stimulating pulses, exhibiting the saturation characteristics of LTP. In addition, the resistance of the device can be flexibly increased or decreased by nearly two times using the testing scheme.

Taking advantage of the continuously adjustable resistance, one single-memristor device has been programmed to 18 designated resistive states to show excellent programmability and demonstrate the superb stability of the device. As shown in Figure 2h,i, the memristor has been precisely programmed into 18 resistive states uniformly distributed in the range of 100–900 Ω and 1000–9000 Ω . Note that the memristor undergoes a 10^5 s retention test after programming to the designated resistive state. After 18 iterations of repeated programming and a total of 1.8×10^6 s (500 h) of retention measurements, the memristor

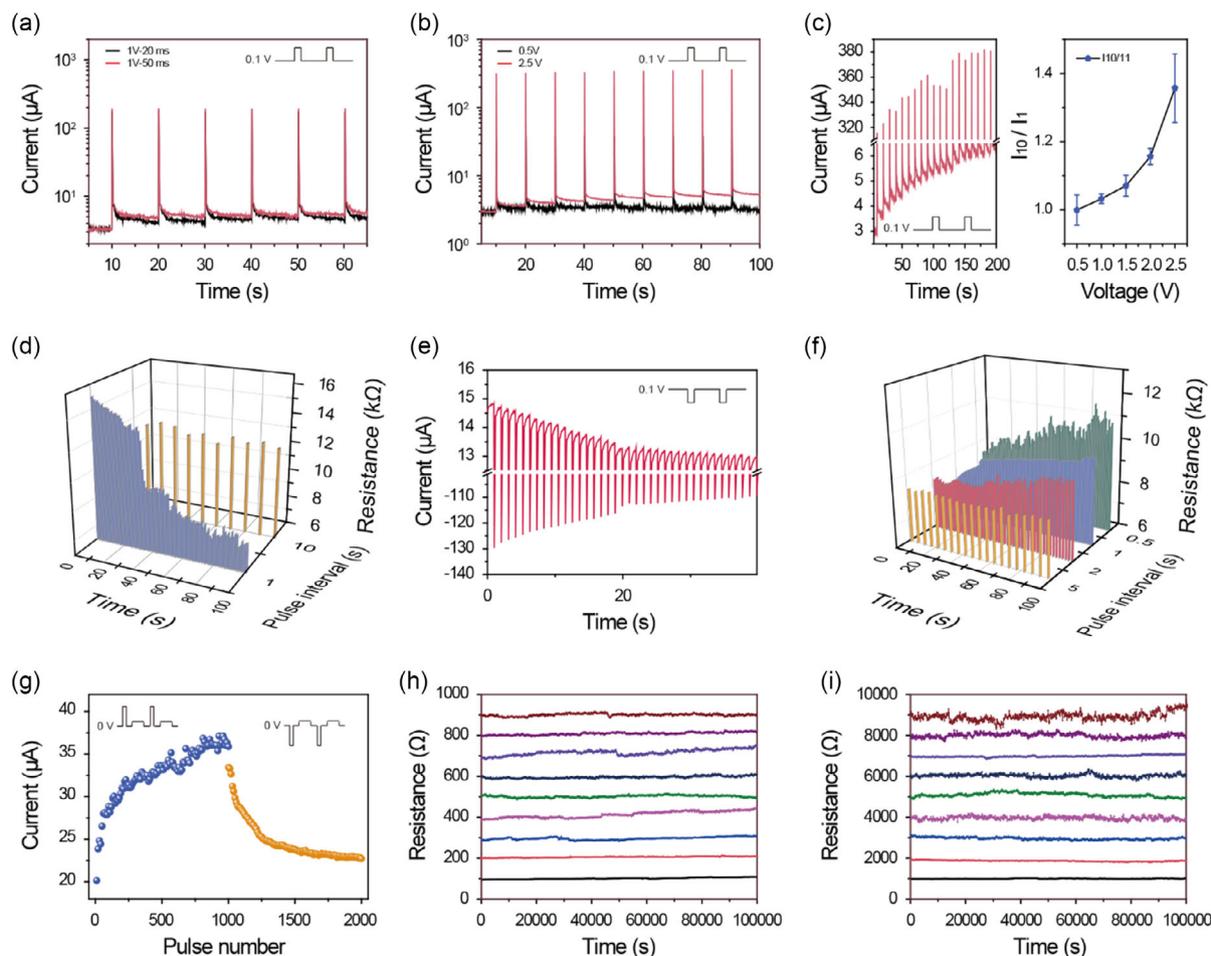


Figure 2. Electrical-tunable synaptic characteristics. a) Pulse-duration-dependent STP with a voltage amplitude of 1 V. b) Pulse-voltage-dependent STP with a pulse duration of 50 ms. c) Left: the excitatory postsynaptic current (EPSC) of the artificial synapse using positive pulses (2.5 V, 50 ms duration with 10 s interval). Right: I_{10}/I_1 with different pulse amplitude, 50 ms duration, and 10 s interval. d) Resistance evolution of the synapse with different pulse intervals and 1 V pulse amplitude. e) The inhibitory postsynaptic current (IPSC) of the artificial synapse using positive pulses (−1 V, 50 ms duration with 1 s interval). f) Resistance evolution of the artificial synapse with different voltage amplitudes. g) Synaptic potentiation and synaptic depression triggered by electric stimuli. The pulse duration is 10 ms and the pulse interval is 500 ms. h) Stability of nine typical LTP states within the range of 100–900 Ω . The resistance is monitored by a DC bias voltage of 1 mV. i) Stability of nine typical LTP states within the range of 1000–9000 Ω . The resistance is monitored by a DC bias voltage of 1 mV.

performance showed no degradation, and the maximum relative deviation observed during the state retention measurements was less than 7%. Furthermore, in Table S1, Supporting Information, multistate programmability and retention stability of state-of-the-art perovskite memristors reported in the literature have been used to benchmark the performance of the memristors fabricated in this work, showing that the polycrystalline MAPbCl₃ NW memristors can provide much more reliable nonvolatile memory states with relatively low current density.^[42–45]

Memristors with stable and programmable multilevel resistive states are highly desirable in the hardware implementation of neuromorphic computing networks. In addition, a memristor is a typical in-memory computing device for hardware implementation of the vector–matrix multiplication operations. Therefore, implementing ANN using a memristor array enables parallel computing of the interconnections between two perceptron layers, reducing latency and power consumption, and has

the potential to overcome the von-Neumann bottleneck.^[46] To this end, we applied the fabricated MAPbCl₃-NWs-array-based devices as a memristor matrix processing unit (M²PU) to substitute the transition core of an encoder–decoder ANN to realize the function of in-image font conversion.

As shown in Figure 3a, a classic ANN, the encoder–decoder architecture, has been adopted in this work to convert uppercase letters to their lowercase fonts.^[47] The method to train the encoder–decoder ANN has been described in detailed in Figure S2, Supporting Information, and related part.^[42,48] The uppercase letters are 6 × 6-pixel images, which are flattened into a 36D vector as the input of the ANN, and preprocessed by the encoder layers into a 4D vector. Subsequently, electrical signals correspond to the 4D data are processed by the 4 × 4 M²PU and output the 4D data to the decoder layers. Finally, the decoder part output a 36D data vector and reshaped it as 6 × 6 image array of the corresponding lowercase letters.

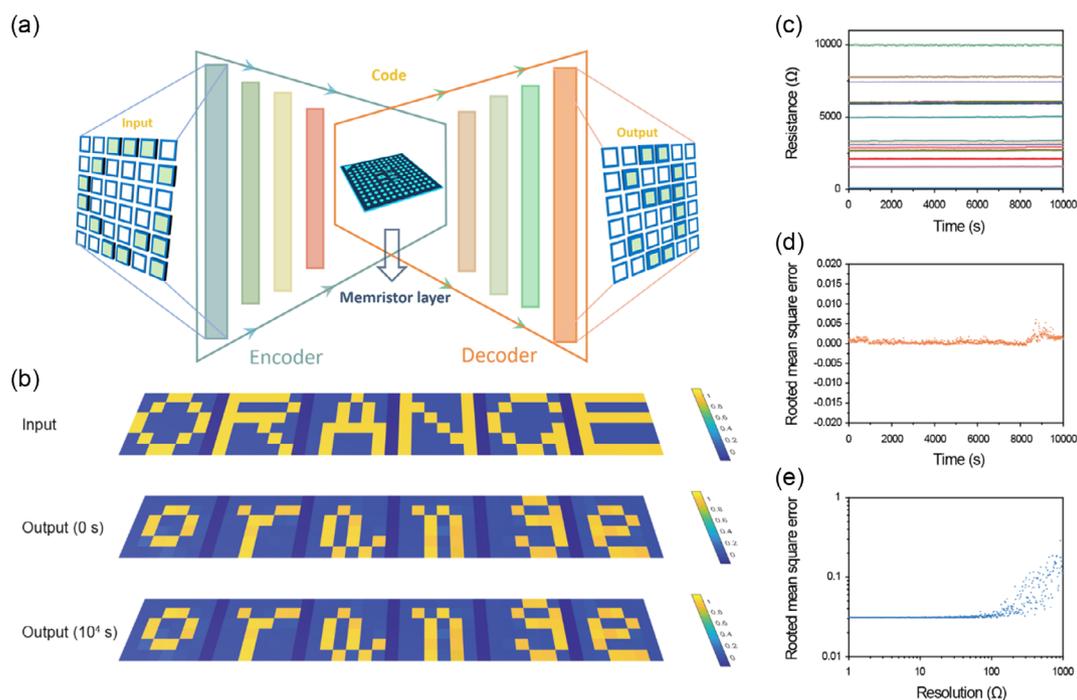


Figure 3. In-image font conversion using IZO/MAPbCl₃ NWs/Al-memristor-array-based matrix process unit. a) The architecture of font style transfer, with encoder (left part) and decoder (right part). b) The input train and validation dataset, choose “ORANGE” as an example. Capital letters (up) are fed into the encoder, and the transferred lowercase letters are output by the memristor neural network (middle: 0 s, bottom: 10⁴ s). c) Stability of 16 neural weights mapped by the encoder–decoder network. d) The relative RMSE between the experimental and simulation versus the test time. e) The RMSE versus resolution of resistance of memristor array. The x axis represents the resistance of memristor can only be the integral multiple times of this value.

Figure 3b shows the experimental results for an example of converting six uppercase letters, “O R A N G E,” to the lowercase “o r a n g e” using an ANN with M²PU. The results show that the converted lowercase letters are recognized in sharp contrast with the background, and the numerical errors of the pixels can be ignored. Moreover, the accuracy of the in-image font conversion is almost maintained after 10 000 s of measurement. Figure S3, Supporting Information, exhibits the input and output results of 26 letters by the M²PU-based in-image processing.

The high accuracy and reliability of neuromorphic computing are attributed to the high stability and precise programmability of the memristors. As shown in Figure 3c, resistive states of the 16 memristors have been precisely programmed to corresponding weight values of the trained ANN, ranging from 100 Ω to 10 kΩ. The distribution of target weight values from the trained results is shown in Figure S4, Supporting Information. It is worth noting that these resistance states are not uniformly distributed in the memristor resistance programming range. Therefore, the computation accuracy achieved using a single-memristor device can be equivalent to that achieved by a multi-bit digital circuit, simplifying the circuit’s complexity and improving computational efficiency.^[46,49] In addition, the M²PU demonstrated here achieves high-precision weighted computations between two perceptron layers of an ANN and can further realize hardware implementation of the fully connected layers of offline-trained ANN through large-scale integration of the polycrystalline NW perovskite memristor on a chip.

To program the weights of the artificial synapse, the pulse number, duration, interval, and amplitude have a combined influence. Figure S5, Supporting Information, gives an example of a typical programming method of tuning the artificial synapse weights by the pulse amplitude. The output accuracy of the M²PU-processed result relative to the theoretically simulated result of ANN is indicated by the root-mean-square error (RMSE) in Figure 3d. The in-image font conversion results exhibit an initial RMSE of 0.118% and end with an RMSE of 0.121%, showing excellent stability. The RMSE of the M²PU-processed results and the ideal output which only has two output states of 0 and 1 is shown in Figure S6, Supporting Information, which indicates <4% resolution error compared to the ideal case.

In addition, we show the importance of programmed resistive states of high precision on ANN computation accuracy. Though ANN models are usually robust to small variations in weights and activations,^[50] programming the resistive states of many memristors to a stable and acceptable resolution close to the corresponding weight remains challenging.^[22,27,51] The ANN model errors related to the resistive-state resolution are plotted in Figure 3e, showing that for a target resistance of 10 kΩ, deviations beyond 200 Ω, or 2% relative, begin to result in severe degradation in model accuracy. Therefore, the memristor with precisely controllable resistive states demonstrated in this work is of vital importance to enable accurate and reliable neuromorphic computing.

Memristors with MAPbCl₃ switching layer and inert IZO and Al electrodes operate in sync with the VCM.^[10,26] The dynamics

of such VCM-based memristor has been modeled to have a vacancy-based conducting filament (CF) while valence ions accumulate near the anode.^[25,26,52] Similarly, the CF in the MAPbCl₃-based switching layer is composed of chlorine vacancies (V_{Cl}^+), and most of the chlorine ions (Cl^-) are driven to the anode electrode by the initial forming process. However, these device models are based on memristors with uniform switching layer structures, such as single crystal or amorphous materials. In perovskite materials with GB structure, theoretical simulations show that mobile valence ions can be confined within the grains or trapped in the GBs while crossing the GBs requires higher activation energies.^[33,34,53] Such a phenomenon may lead to uncommon mechanisms and performance of memristors.

High-resolution transmission electron microscope (HRTEM) image of a MAPbCl₃ NW and its fast Fourier transform (FFT) pattern are shown in Figure 4a, indicating a polycrystalline structure. In particular, we have characterized that the size of perovskite nanograins exceeds 10 nm under HRTEM, thereby these NWs with a diameter of only ≈ 15 nm is likely to have horizontal GBs transverse the entire NW. Hence, as shown in Figure 4a, polycrystalline MAPbCl₃ NWs are modeled as having a structure with multiple nanograins stacked on top of each other and forming horizontal GBs that cut the NWs. Such a device structure not only provides a multilevel reservoir for Cl^- ions, but also prevents the drift diffusion of V_{Cl}^+ in the resistive switching layer.

To build a theoretical ground for device operation principle, the activation energies for migration of Cl^- and V_{Cl}^+ in the grain and across the GB have been computed using the first-principles-based nudged elastic band (NEB) method in the Quantum Espresso code.^[54] Figure 4b plots the two examples of computed atomic trajectories of Cl^- moving in the perovskite nanograin and into the GB.

The computed activation energy profiles along movement trajectories of Cl^- and V_{Cl}^+ are plotted in Figure 4c. The results show that the migration of V_{Cl}^+ in grain requires an activation energy of about 0.53 eV, while the activation energy for Cl^- is only about 0.11 eV. Therefore, driven by an electric field, the mobility of V_{Cl}^+ is negligible compared to the drift of Cl^- in the grain. The migration trajectories in NEB simulations are plotted in Figure S7, Supporting Information.

As a result, Cl^- can move more freely in the grains, resulting in a more uniform V_{Cl}^+ distribution in the grains and captured by the GB in a more uniform manner. In comparison, the CF composed of V_{Cl}^+ is less mobile, resulting in stable device retention performance.

In fact, VCM-based memristors with multilayer structures have shown enhanced stability and programmability. This can be attributed to the reduced local heating effect in such a device structure using a diffusion barrier layer to make the distribution

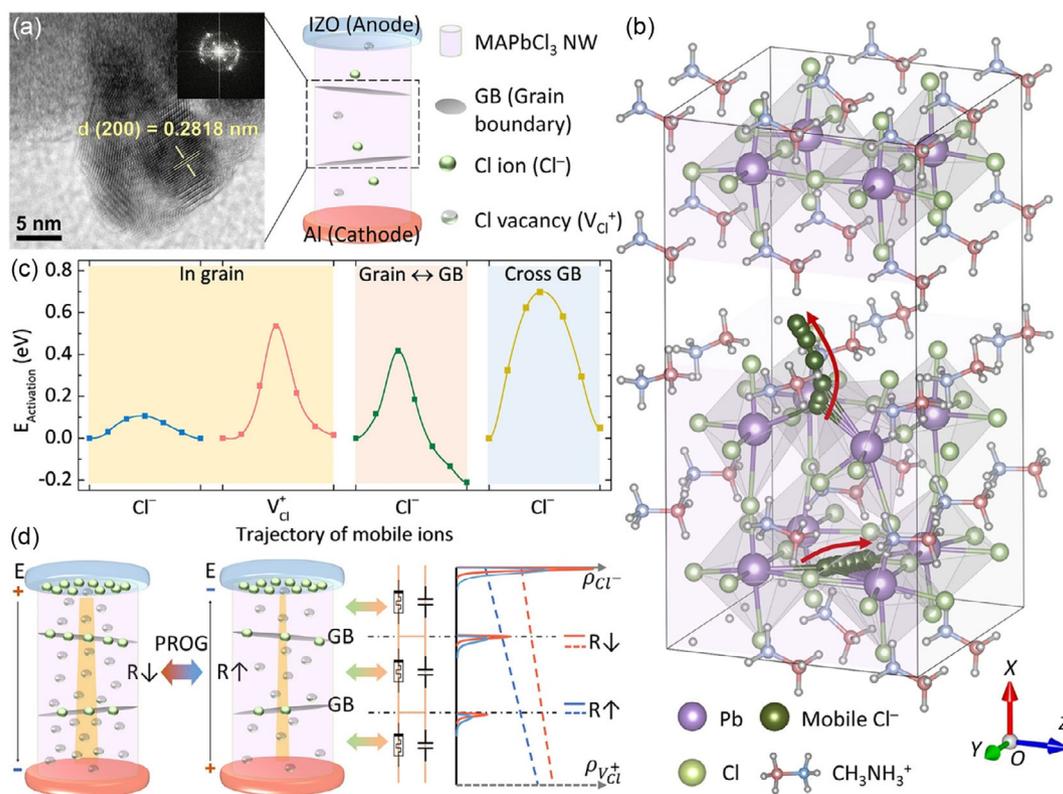


Figure 4. First-principles simulations of operation mechanism of polycrystalline MAPbCl₃-nanowires-array-based memristor. a) HRTEM image of the polycrystalline MAPbCl₃ nanowire showing varying lattice orientations and corresponding fast Fourier transform (FFT) analysis. b) Exhibition of two movement trajectories of Cl atoms in the MAPbCl₃ crystal structures obtained by the first-principles NEB simulations. c) The activation energy profile of Cl ions (Cl^-) and Cl vacancies (V_{Cl}^+) along the movement trajectories in MAPbCl₃ crystal structures simulated by the first-principles NEB method. d) A conceptual model of device dynamics of the memristor caused by PROG operations is illustrated.

of CFs more uniform.^[29,31] The polycrystalline perovskite NW memristors fabricated in this work realize a multilevel GB structure, which can disperse and store the Cl^- ions like a multistage reservoir. In addition, this work uses NWs with diameters that are even smaller than the main conduction path observed in many memristors, hence making the conductive paths within the NWs more evenly distributed and greatly weakening the influence of local heating effects.^[29,30] The continuous programmability and high stability advantages of the fabricated vertical polycrystalline NW memristor can be a combined effect of the previously discussed mechanisms.

A conceptual principle for resistive programming (PROG) of the polycrystalline MAPbCl₃ NW memristors is illustrated in Figure 4d. When the device is programmed with multistates, relatively uniform V_{Cl}^+ can be generated in the grains to constitute continuous CF, as shown by the dashed lines in the coordinate diagram. Meanwhile, the Cl^- can be dispersed, captured, and stored in the GB, as shown by the solid curves in the coordinate diagram. The memristor can be modulated to a higher-resistive state by releasing Cl^- from GBs into grains, a process that can be represented by the red solid curves in the coordinates reshaping into the blue solid curves. The released Cl^- can neutralize V_{Cl}^+ concentration ($\rho_{V_{Cl}^+}$) and weaken the CF. This process is represented by the red-dashed line in the coordinate changing to the blue-dashed line. The device mechanism corresponding to programming the memristor into a lower-resistive state can also be demonstrated by reshaping the blue lines to the red lines in the coordinate diagram.

3. Conclusion

This work devised solution-process-synthesized polycrystalline MAPbCl₃ NWs to fabricate memristors aimed at neuromorphic analog processing. Using pulsed-signal stimulations, the fabricated memristors can mimic the short-range plasticity and long-range plasticity behaviors of biological synapses. In particular, the memristors exhibit more than 18 levels of continuously programmable resistive states with a total retention time longer than 1.8×10^6 s. Device structure characterizations and the first-principles simulations indicate that the continuous programmability and high reliability of the fabricated memristors may benefit from the polycrystalline NW structure of the MAPbCl₃-resistive switching layer. Leveraging the ability to precisely control the resistive state of the device, this work fabricated a memristor array to replace one transition layer in an ANN, serving as a matrix processing unit between two perceptron layers. The resistive states of memristors are precisely programmed to the corresponding trained weights in the ANN and enable high accuracy and reliable in-image font conversion.

4. Experimental Section

Device Fabrication: The PAM templates were made from aluminum chips with a size of 15 by 25 mm by using the anodic anodization method which has been reported previously.^[21,55,56] An electro-polishing process by acidic solution (25% HClO₄ and 75 vol% absolute CH₃CH₂OH) needed to be applied first to minimize the roughness of the bare Al chips. Two times anodization processes in 5 vol% H₂SO₄ were followed to form

the ordered NWs array channel. The first time of anodization was etched away by a mixture of phosphoric acid (6 wt% H₃PO₄ and 1.8 wt% CrO₃) at 98 °C. The natural hexagonal ordering was left, which would improve the uniformity of the next anodization. The length and diameter of the PAM channel could be managed by the voltage applied and the time control.

We have observed that synthesizing NWs in smaller-diameter PAM channels using the solution process resulted in a monocrystalline quantum-wire structure, while solution-grown perovskite NWs in larger-diameter PAM channels might have multidirectional GBs like those of perovskite thin films because both processes share the same nucleation and growth mechanism of the Ostwald ripening model.^[57,58] Therefore, to realize polycrystalline perovskite NWs and fabricate reliable and continuously programmable memristors, we chose to use 15 V anodization for 3 min to produce ≈ 70 nm thick PAM template with ≈ 15 nm channel diameter.

The MAPbCl₃ NWs array was fabricated by solvent engineering on the as-fabricated PAM templated. Since chlorine had a stronger electronegativity and formed MAPbCl₃ with a more compact lattice structure, a decent and stable memristor performance was promoted. The precursor solution was prepared by CH₃NH₃Cl and PbCl₂ dissolving in dimethyl sulfoxide (1.1 g mL⁻¹) with a 1:1 molar ratio before being spin-coated on PAM. Annealing at 110 °C for 10 min was followed to help the crystallization of MAPbCl₃ NWs. The top electrode (IZO) was deposited by a radio-frequency sputtering process under the condition of ≈ 0.23 Pa and 200 W. The electrode area was 0.785 mm². Wire bonding and norland optical adhesive 81 epoxy packaging were carried out to package the device.

Material Characterization: The cross-section STEM image of the MAPbCl₃ NWs array was obtained by an FEI Helios Nanolab 600i dual-beam, focused-ion-beam, and field-emission-gun scanning electron microscope. The STEM-EDX data with STEM high-angle annular dark-field mode was acquired by an FEI Talos TEM with Super-X EDX. High-resolution TEM was carried out by TEM JEOL (2010). A Bruker D8 X-Ray 22 diffractometer was employed to perform the XRD characterization.

Electrical Measurements: The basic electrical characterization including I–V characterization and pulse-dependent performance was performed by Keithley 2450 source meter and home-built LABVIEW programs. The 4 × 4 memristor array implementation of in-image font conversion processing was achieved by National Instruments Controller PXI 8301, Multiplexer PXI 2530, SMU PXI 4130, and Keithley 2450 in conjunction.

First-Principles-Based NEB Simulation: The first-principles simulations conducted in this work were performed using Quantum Espresso with the projected augmented wave approach. The generalized gradient approximation Perdew–Burke–Ernzerhof was adopted for the exchange–correlation functional. The Brillouin zone was sampled by a 3 × 3 × 3 Monkhorst–Pack grid, and the energy cutoff was set to 60 Rydberg. All geometry structures were fully relaxed until the convergence criteria of energy and forces of 10⁻⁶ and 0.003 Ry Å⁻¹ were reached, respectively. All energy cutoff and k points were tested until the energy reaches its convergence. The fully optimized structures were used as the initial configurations for the subsequent calculations.^[59] The barriers for the Cl ion and vacancy migration in cubic MAPbCl₃ structures were calculated using the climbing NEB through Quantum Espresso codes. During the NEB calculations, all the atoms were relaxed in xyz dimensions, and the simulations reached convergence with forces less than 0.05 eV Å⁻¹ for each transition structure.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

artificial synapses, nonvolatile multistates, perovskite memristors, vertical nanowires array

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